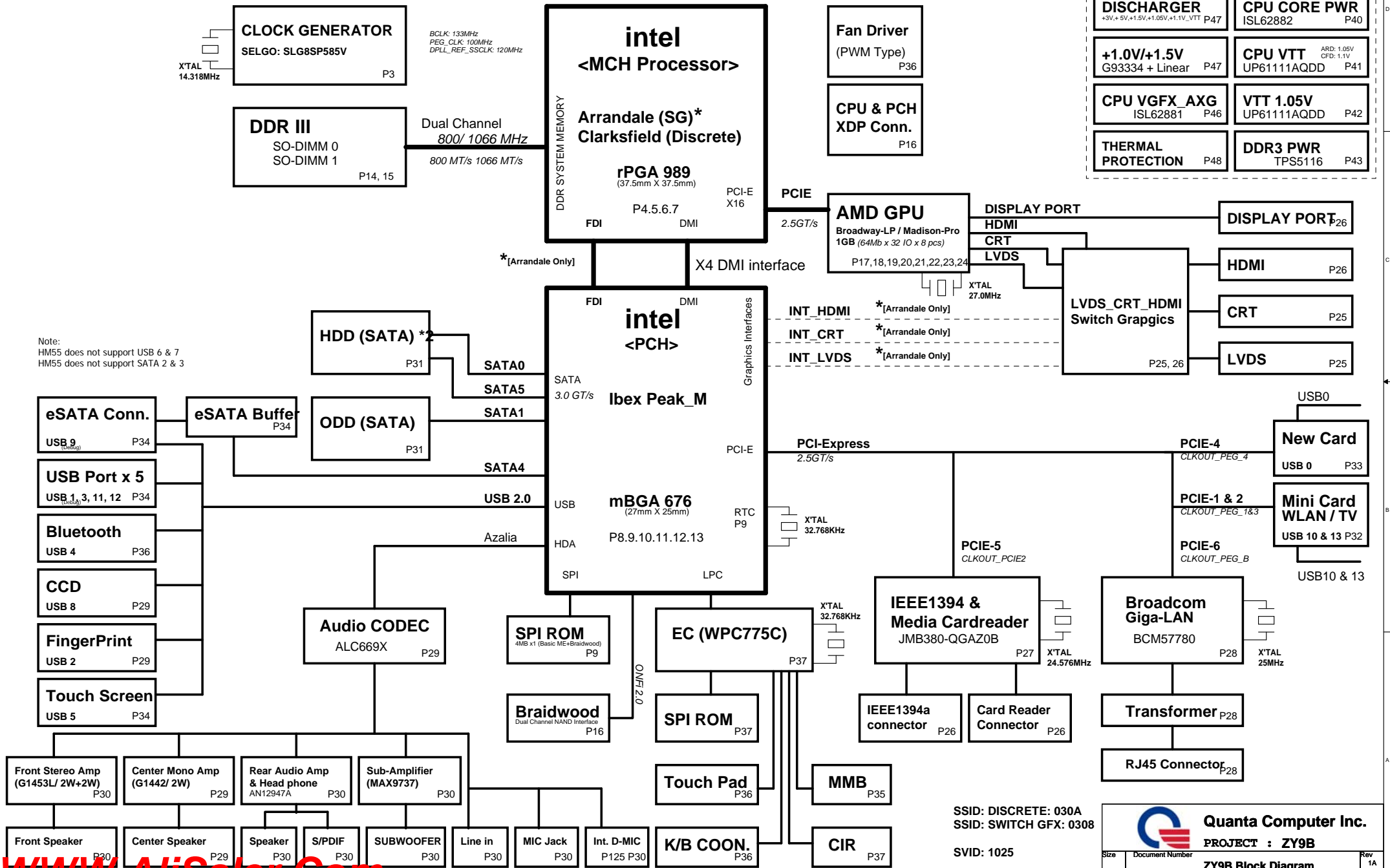
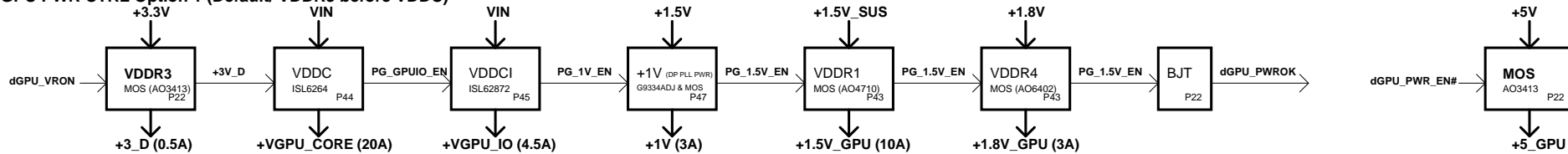


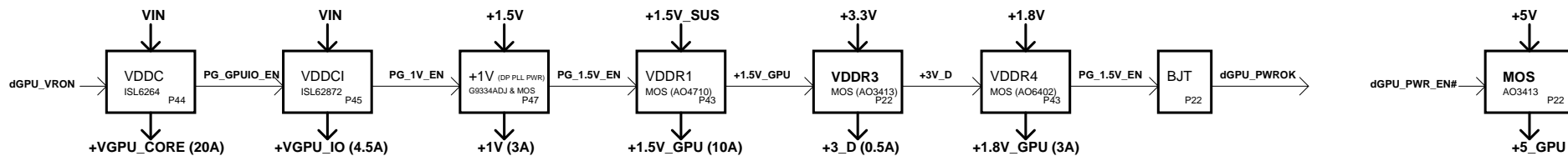
ZY9B SYSTEM BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



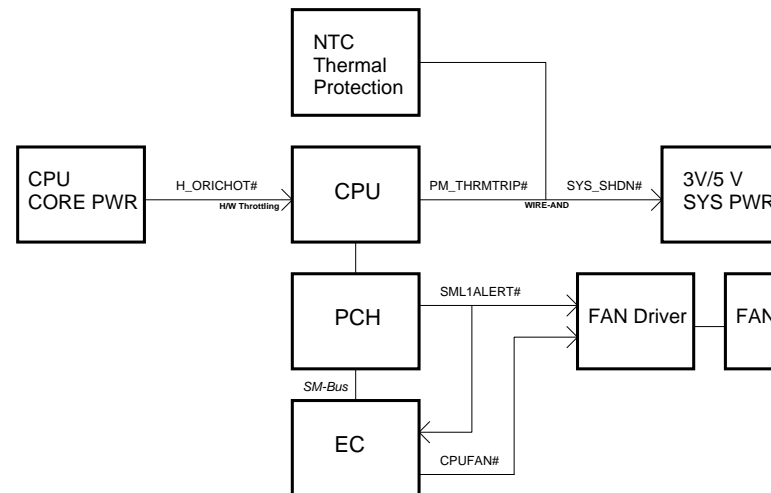
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

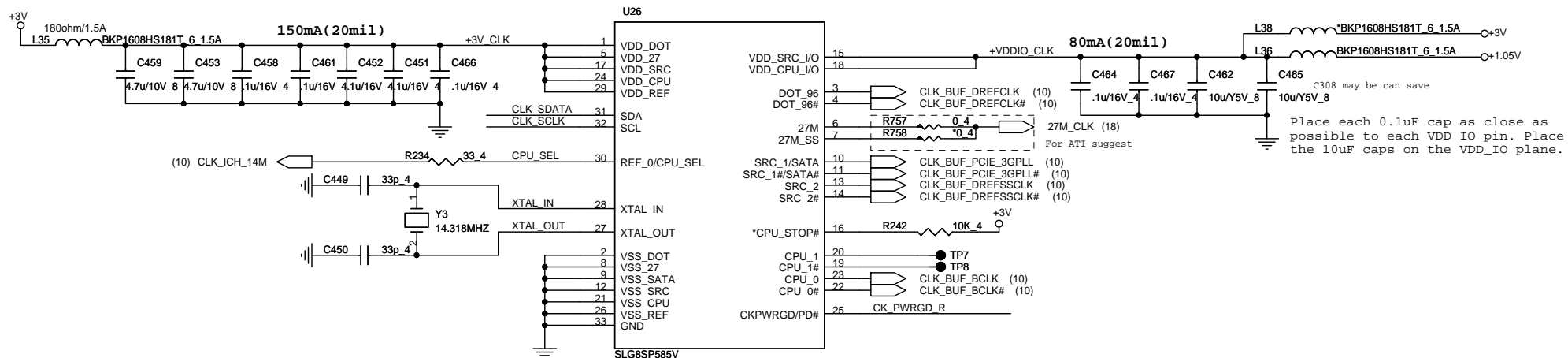


Power States

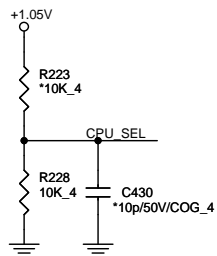
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



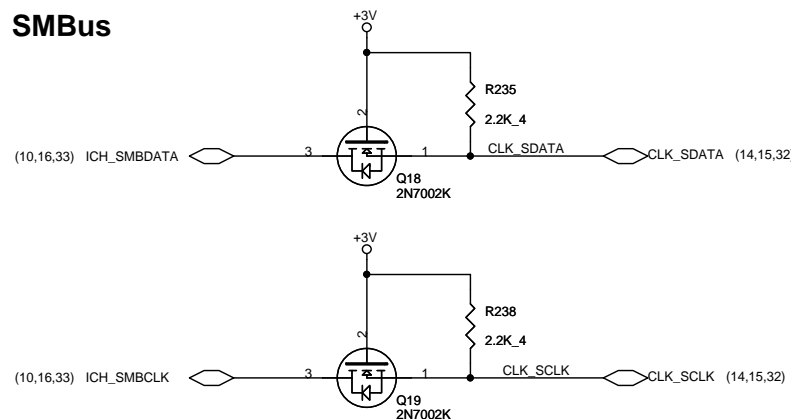


CPU_CLK select

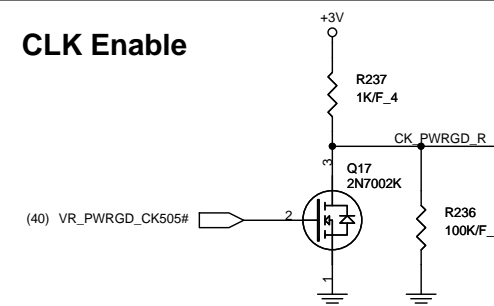


CPU_SEL	0	1
CPU0/1=133MHz (default)		CPU0/1=100MHz

SMBus



CLK Enable

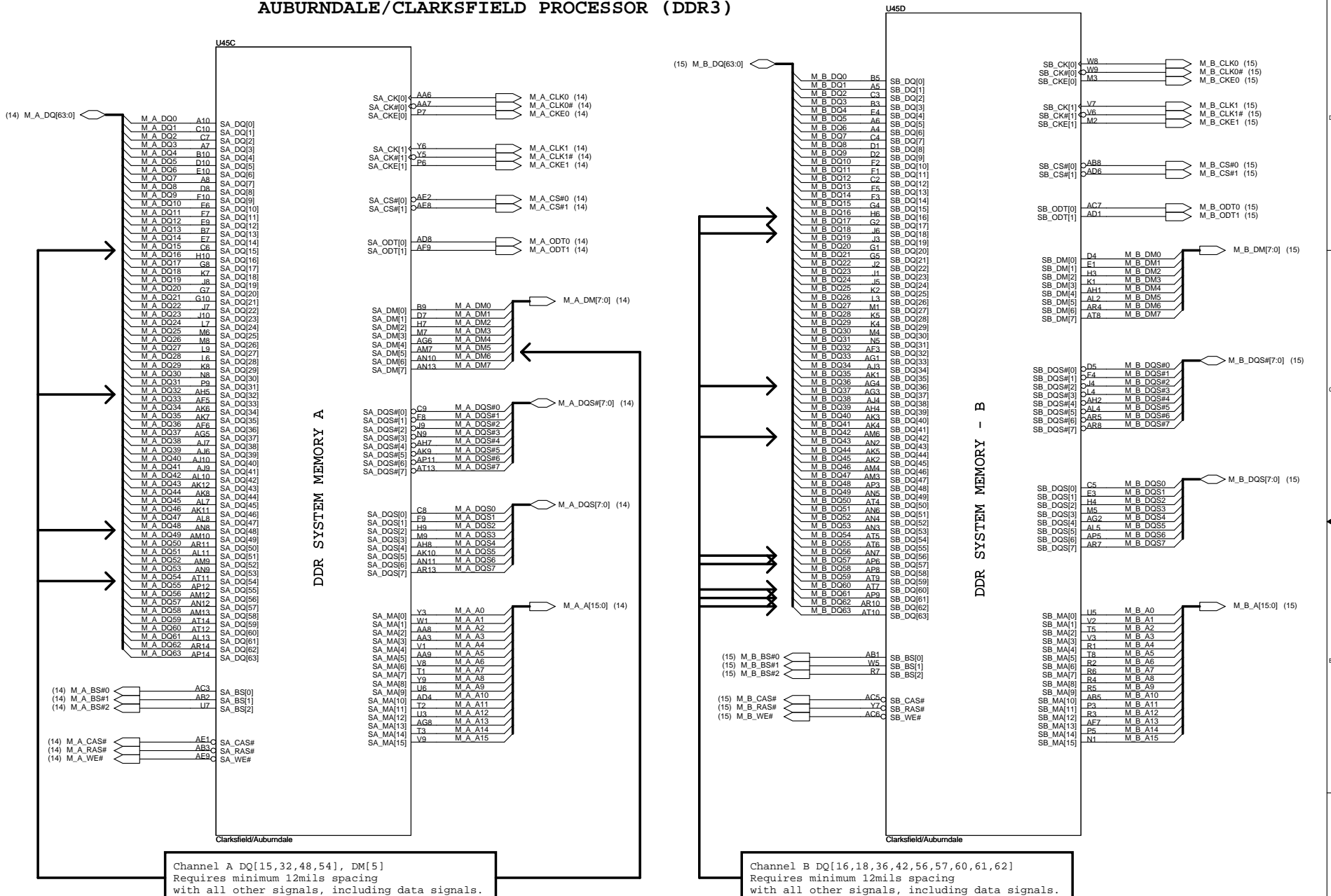


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PROJECT : ZY9B

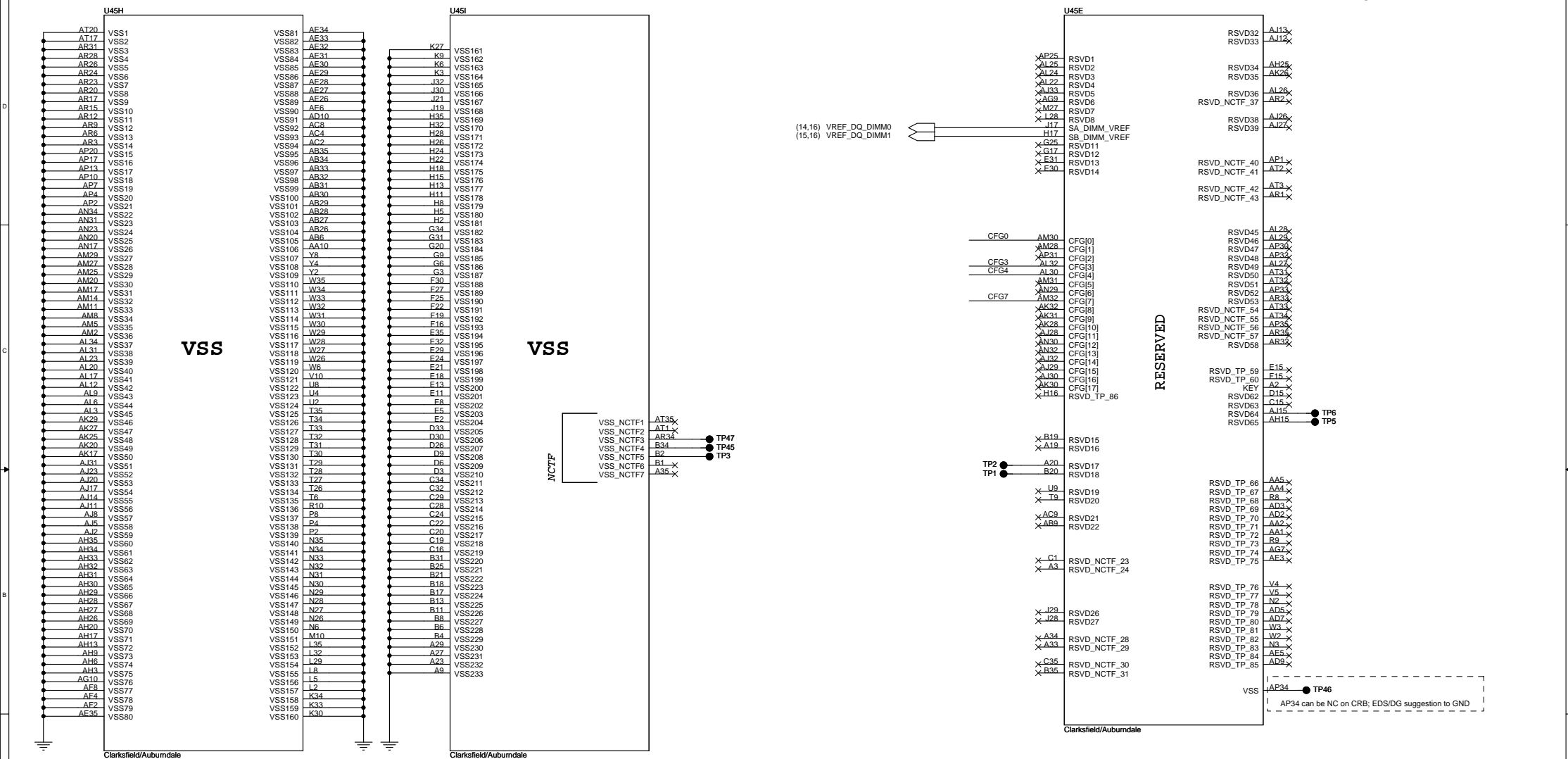
Size	Document Number	Rev
	Clock Generator	1A
Date:	Thursday, September 17, 2009	Sheet 3 of 49

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

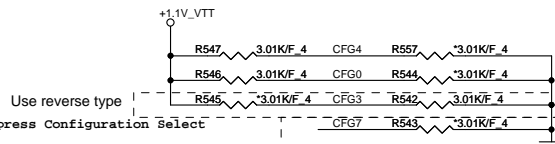
AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed. (ES1 only)

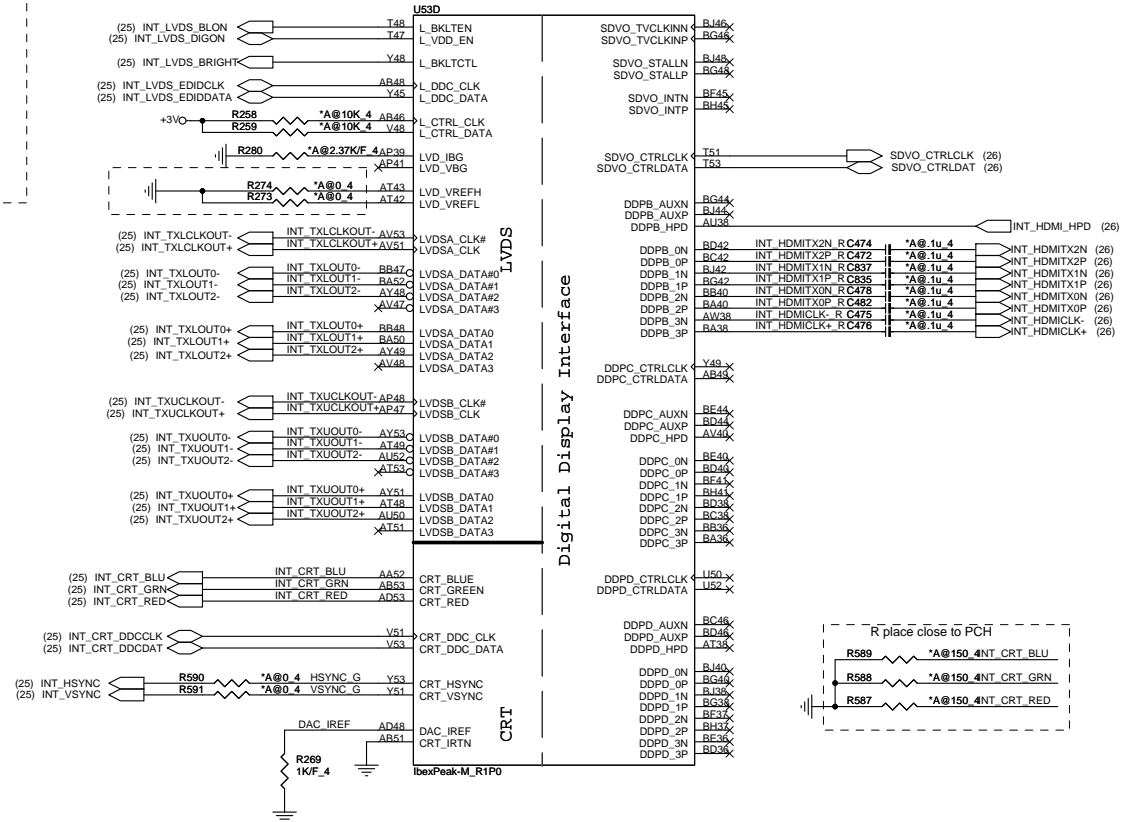
Quanta Computer Inc.
PROJECT : ZY9B

Size Document Number
AUBURNDA 4/4

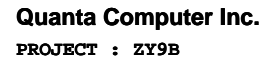
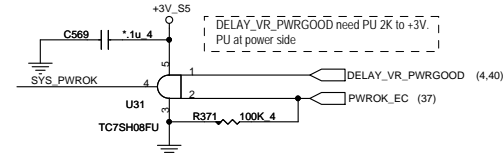
Date: Thursday, September 17, 2009 Sheet 7 of 49

Rev 1A

IBEX PEAK-M (LVDS,DDI)



System PWR_OK



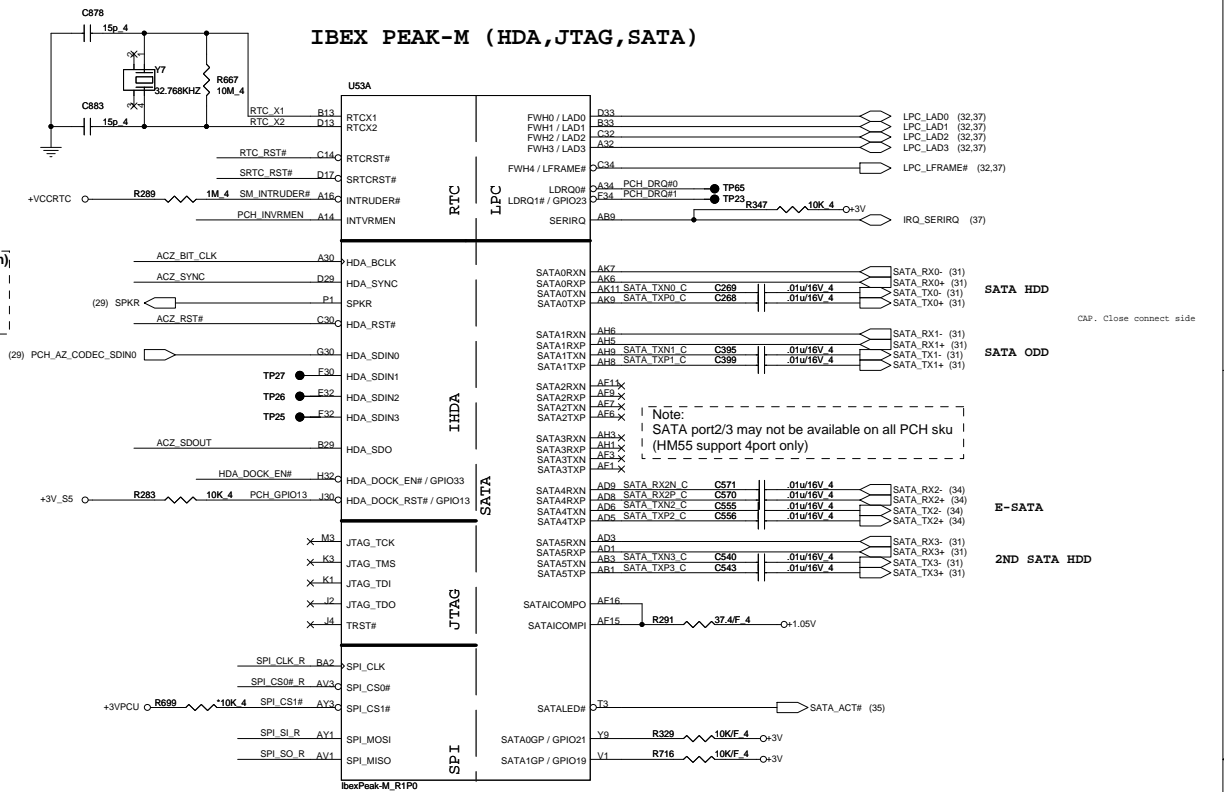
Date: Thursday, September 17, 2009 Sheet 8 of 49

[illegible]


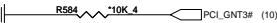
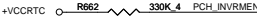
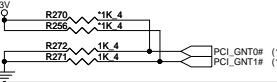
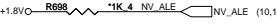
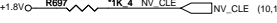
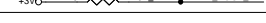

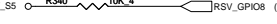
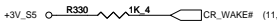
Figure 10 illustrates the recommended termination for ACZ signals. It shows four signal lines, each with a termination resistor connected to a 33.4 ohm ACZ signal source. The components are labeled as follows:

- PCH_AZ_CODEC_SYNC**: Termination resistor **R533** connected to **33.4 ACZ SYNC**.
- PCH_AZ_CODEC_RST#**: Termination resistor **R617** connected to **33.4 ACZ_RST#**.
- PCH_AZ_CODEC_SDOUT**: Termination resistor **R636** connected to **33.4 ACZ_SDOUT**.
- PCH_AZ_CODEC_BITCLK**: Termination resistor **R627** connected to **33.4 ACZ_BIT_CLK**. A capacitor **C845** (27pF) is connected between the resistor and ground.

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

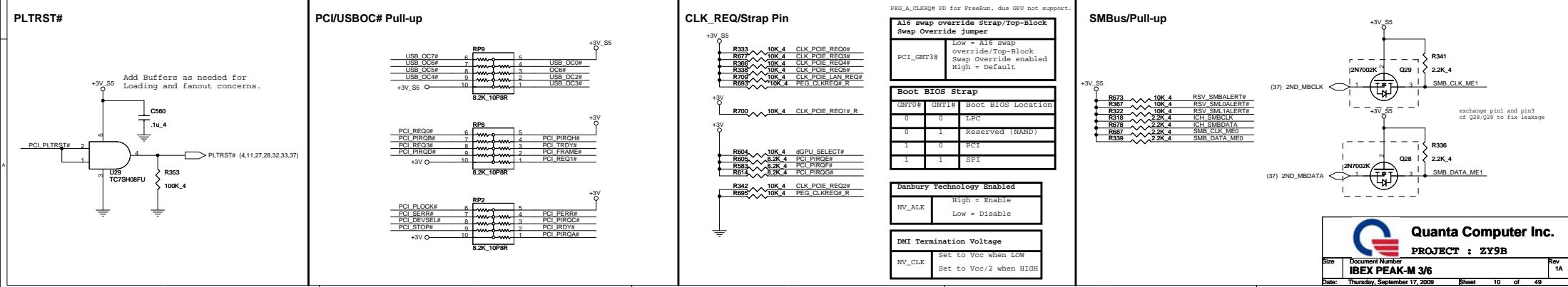
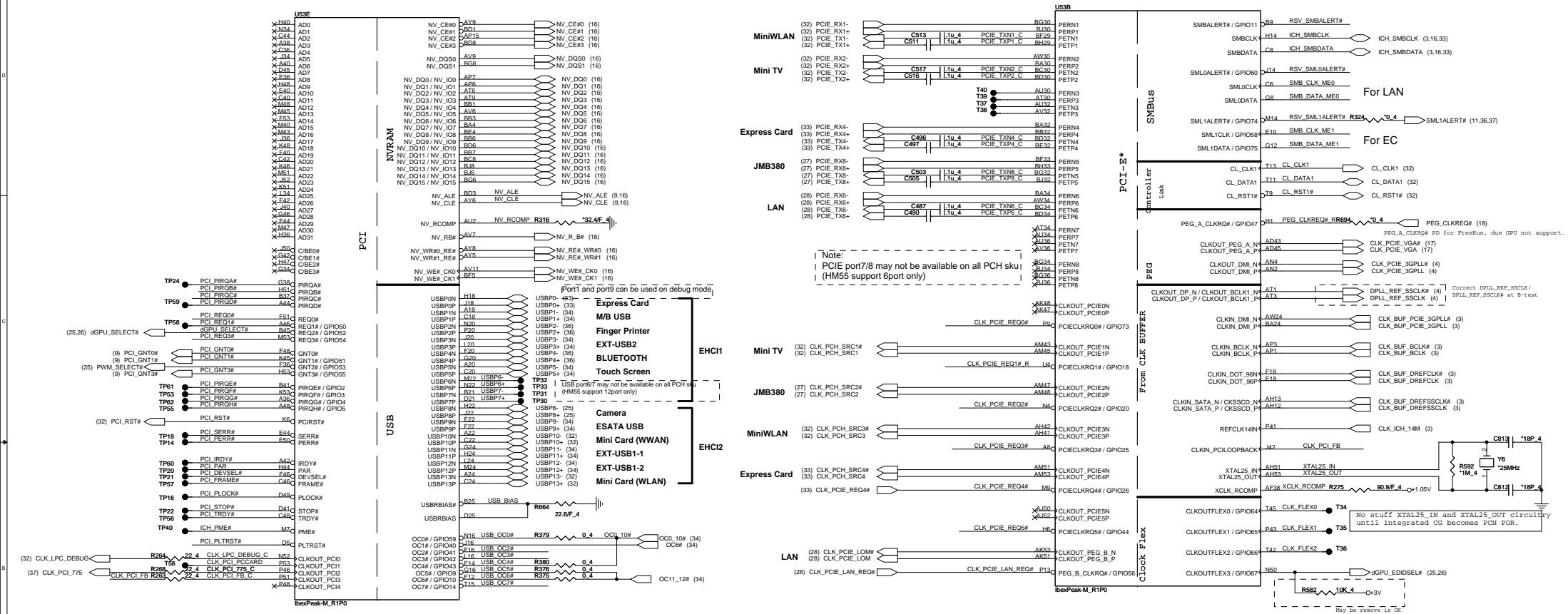


PCH Strap Table

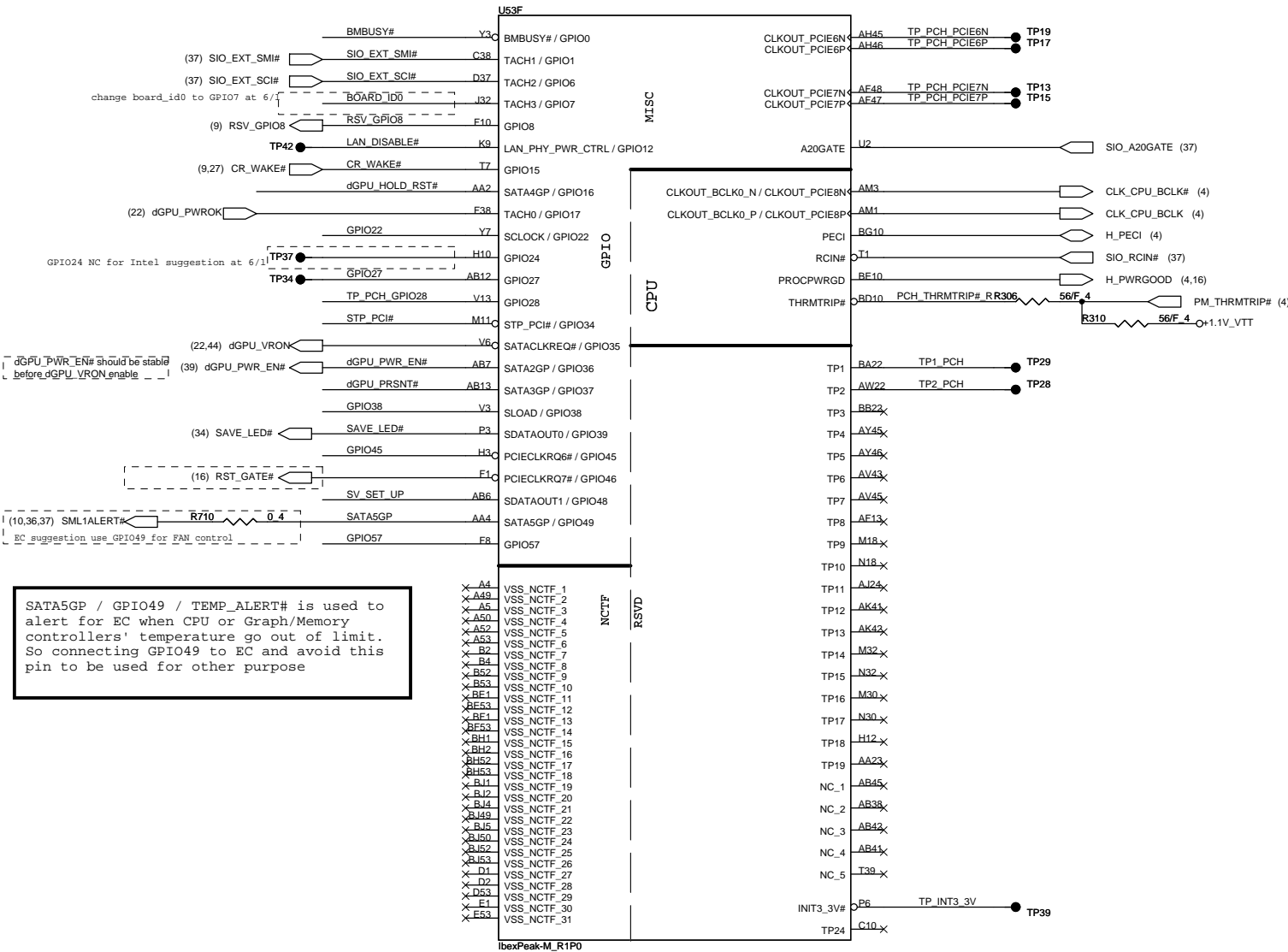
Pin Name	Strap description	Sampled	Configuration	ZY9B note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V _O  SPCR												
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	 PCI_GNT3# (10)												
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC  PCH_INVRMEN												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] 
GNT1#	GNT0#	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK														
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN												
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V _O  NV_ALE (10,16)												
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V _O  NV_CLE (10,16)												
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V _O  HDA_DOCK_EN#												
SPI_MOSI	ITPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V _O  SPI_SI_R												
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)													
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_SS  RSV_GPIO8 (11)												
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)													
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use default (0 = 1.8V supply)												
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_SS  CR_WAKE# (11,27)												

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

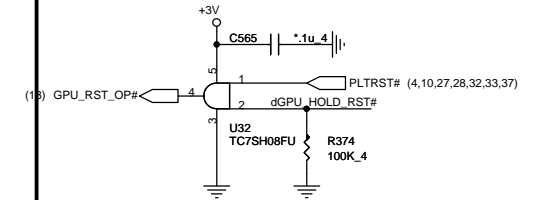


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

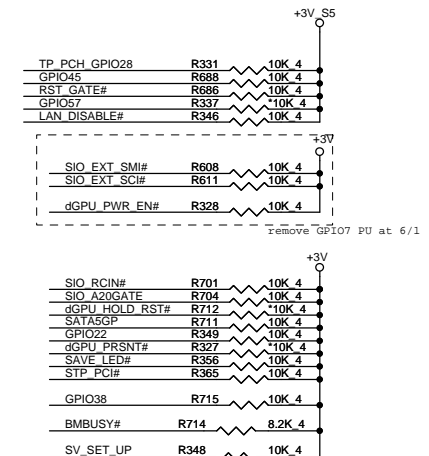


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

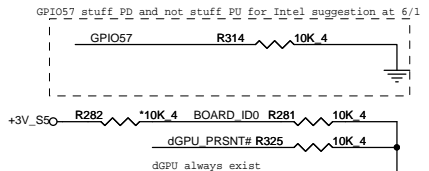
GPU_RST#



GPIO Pull-up/Pull-down



SV_SET_UP 1-X High = Strong (Default)

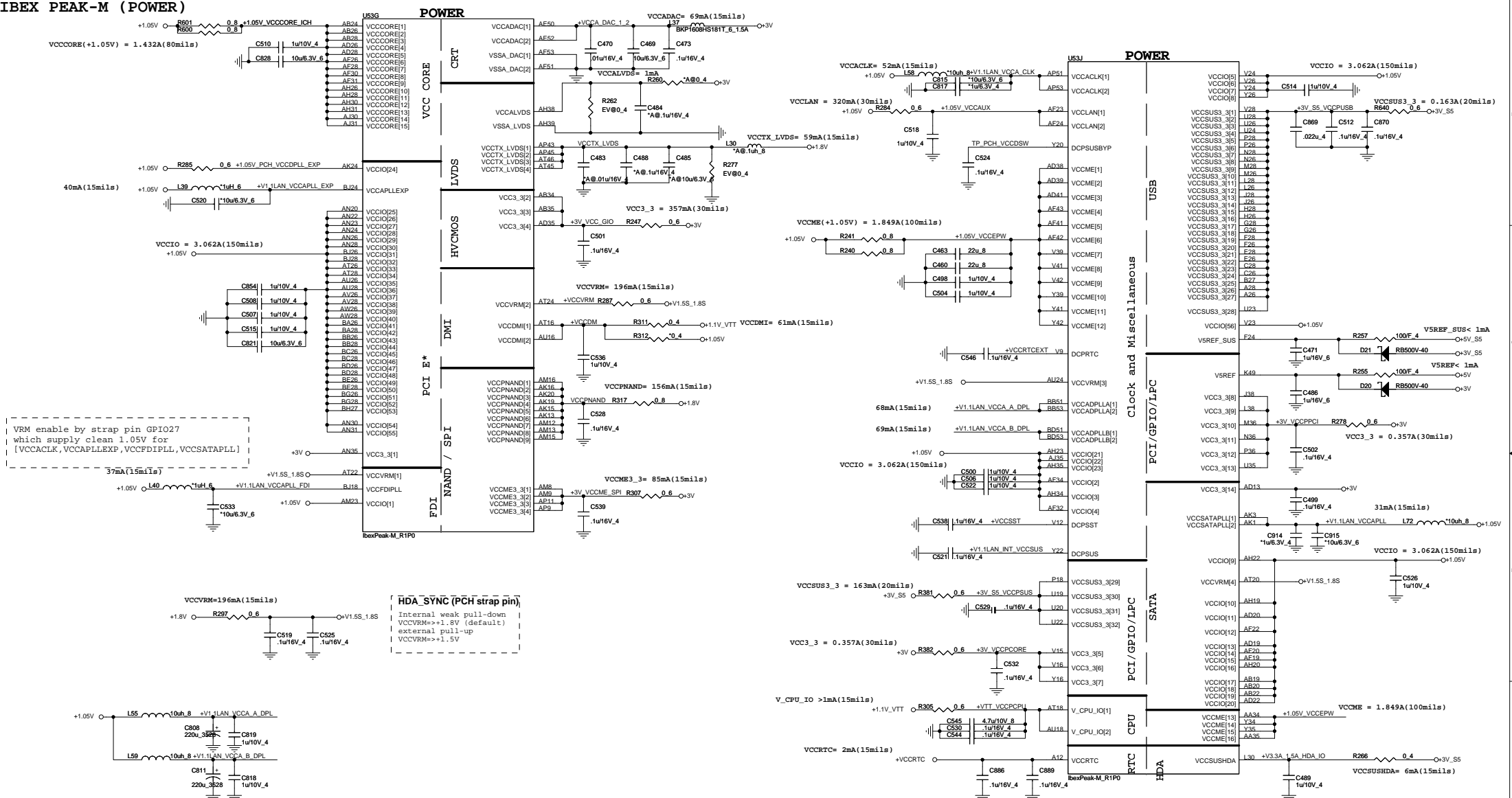


Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

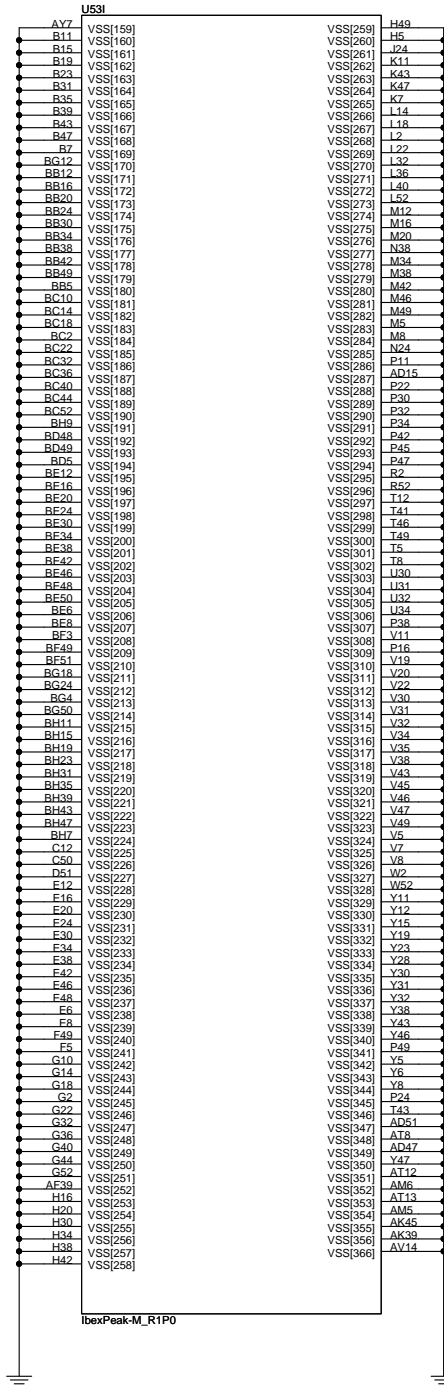
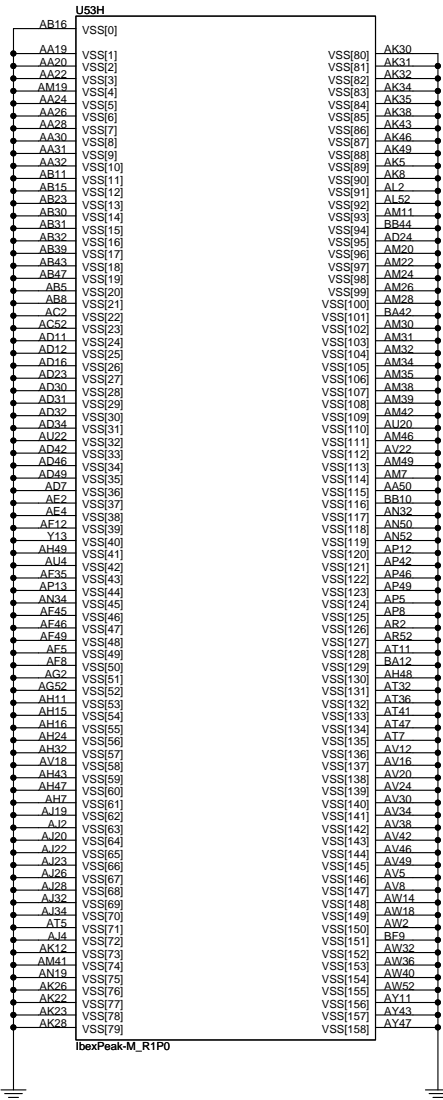


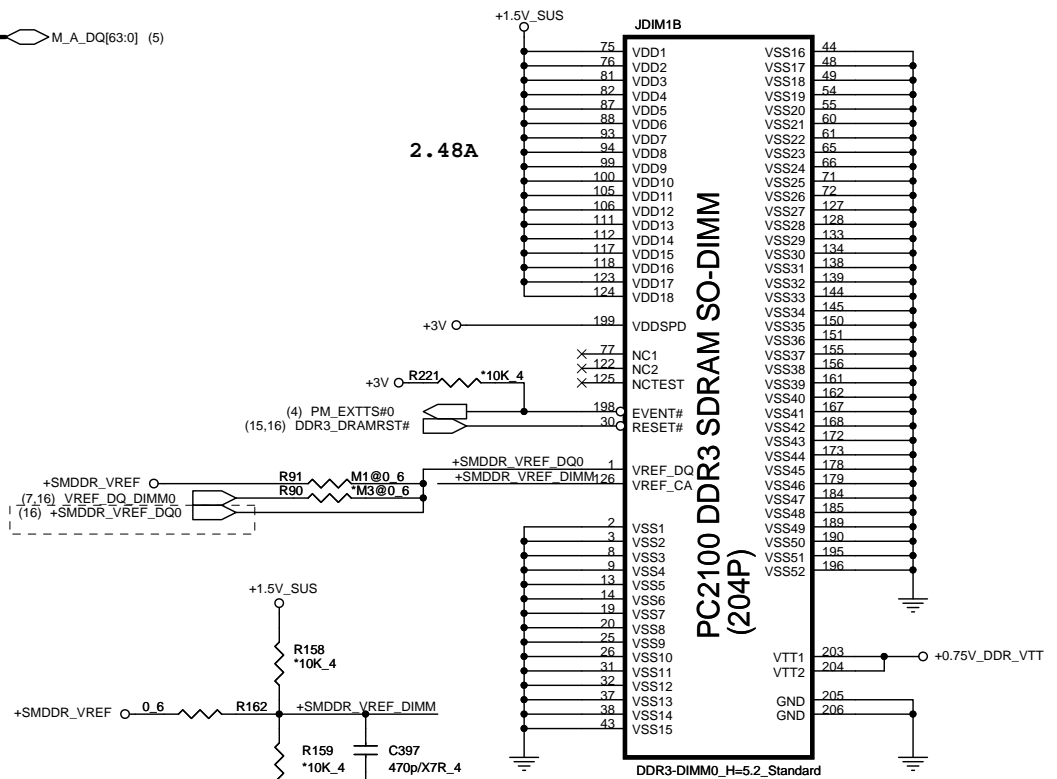
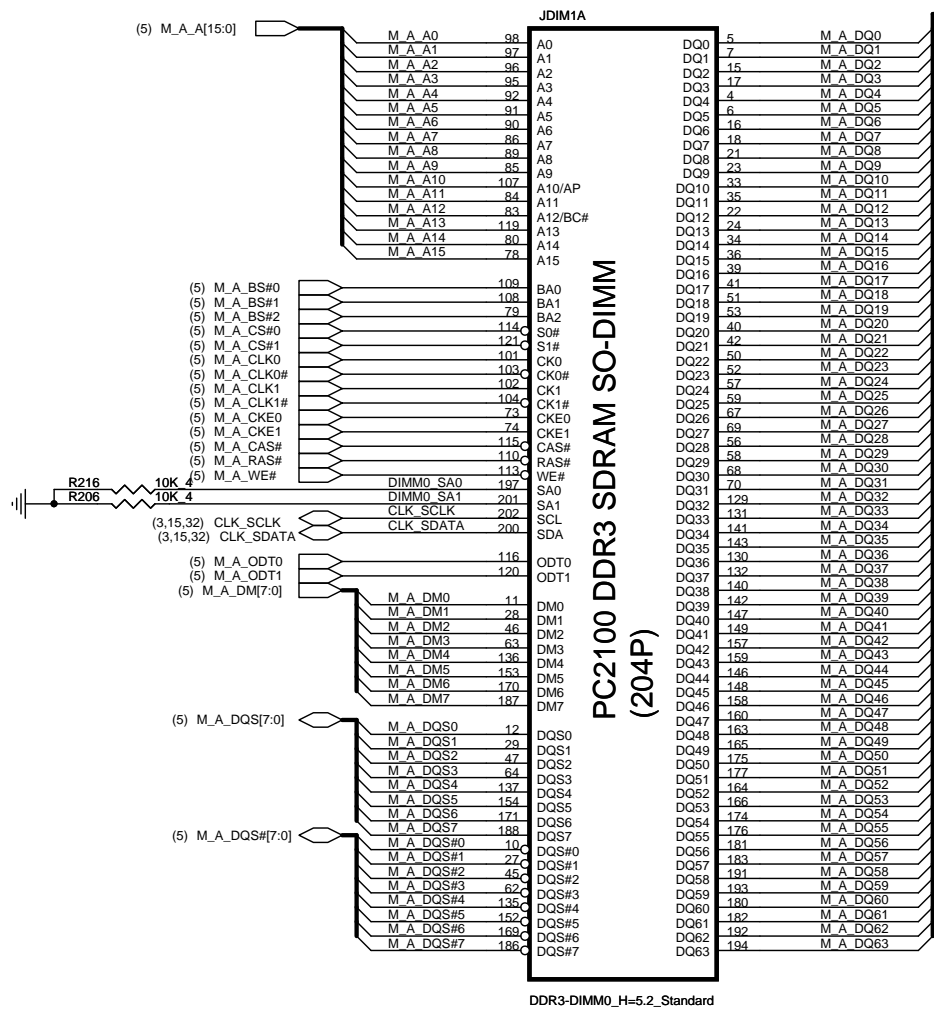
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IBEX PEAK-M (POWER)

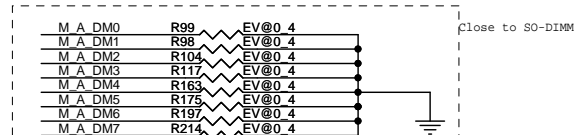
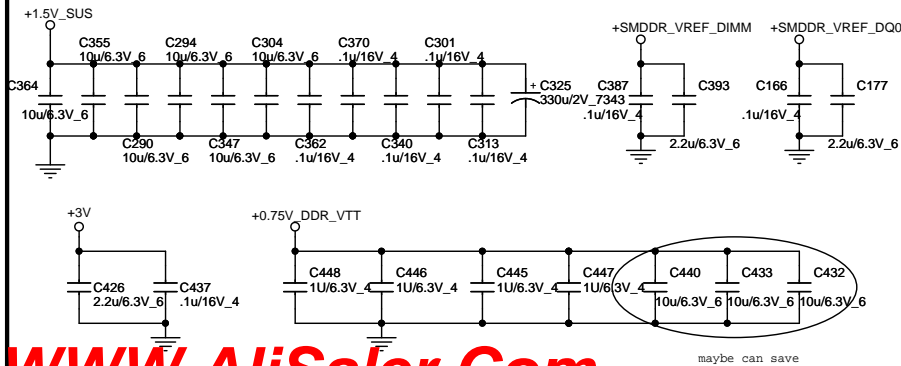


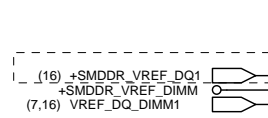
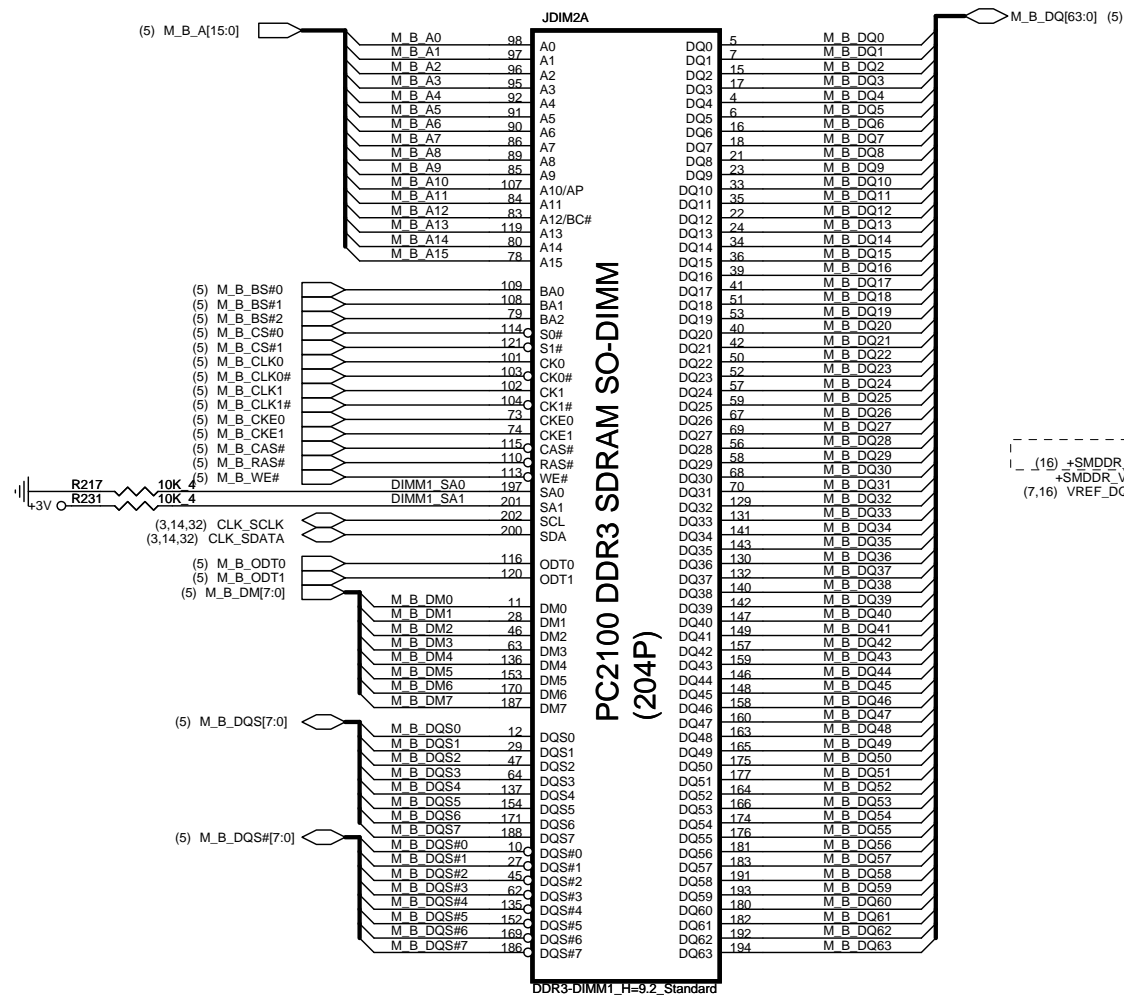
IBEX PEAK-M (GND)



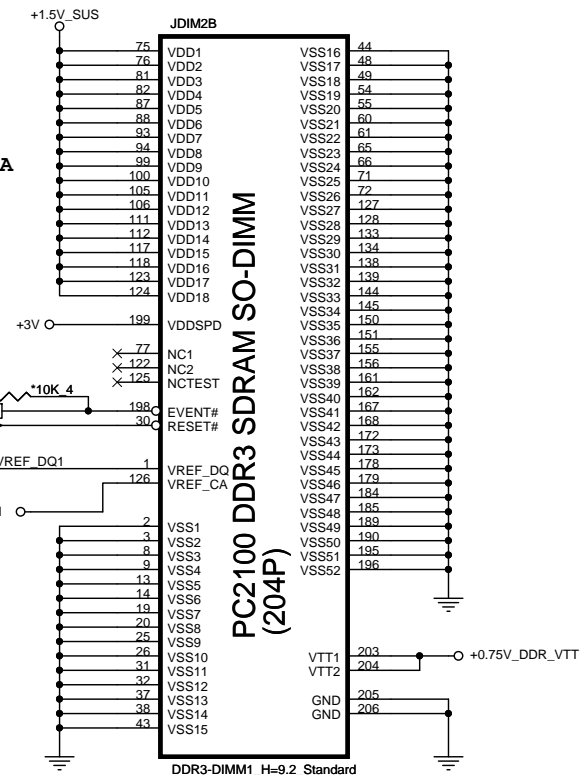


Place these Caps near So-Dimm0.

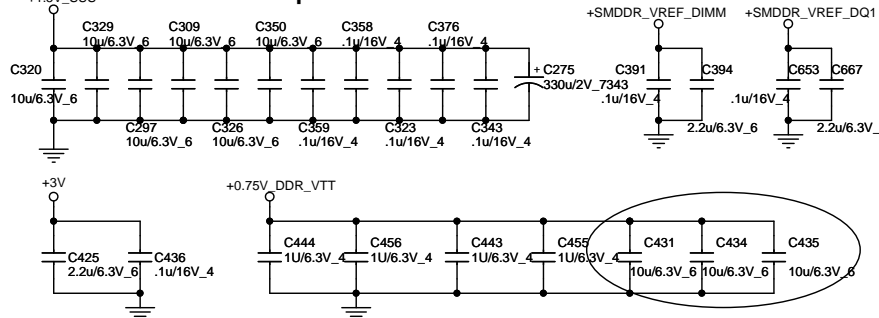




2.48A

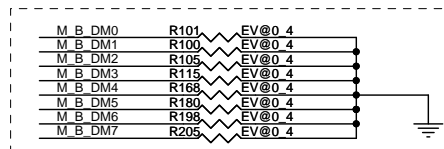


Place these Caps near So-Dimm1.



maybe can save

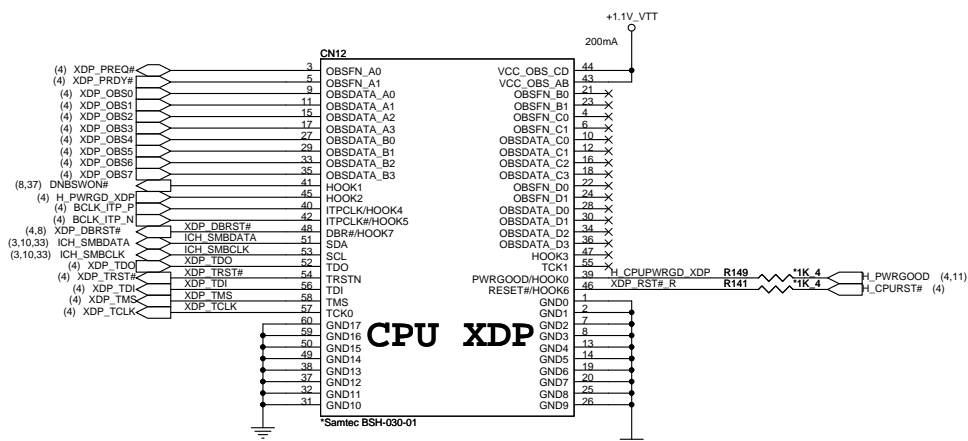
Close to SO-DIMM



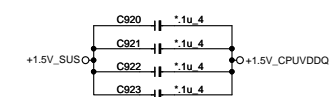
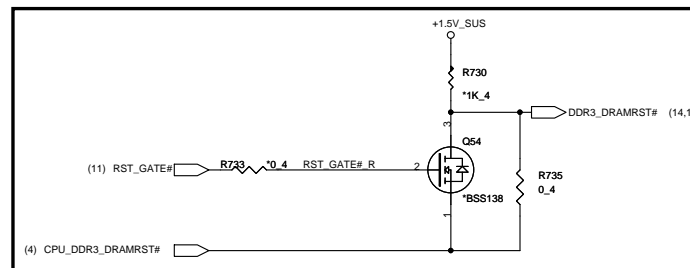
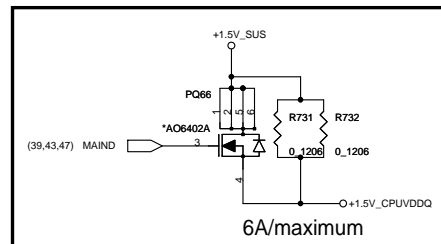
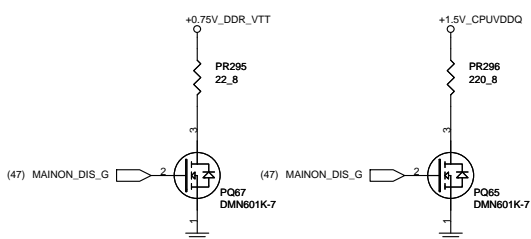
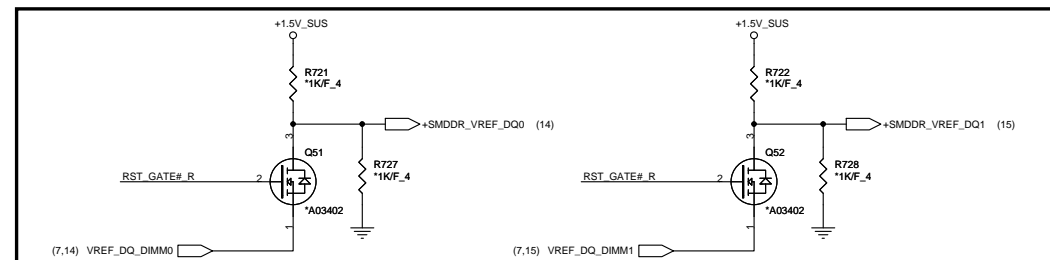
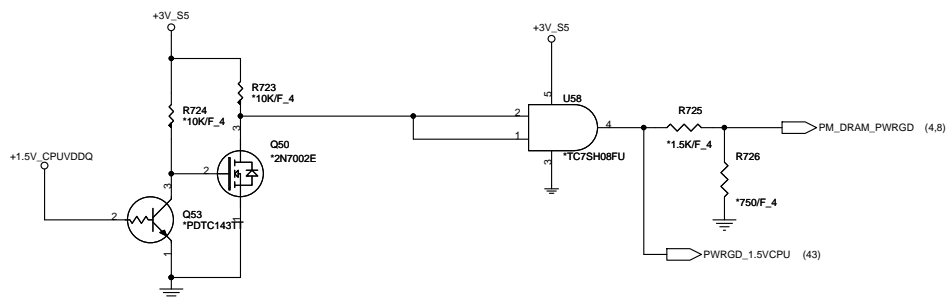
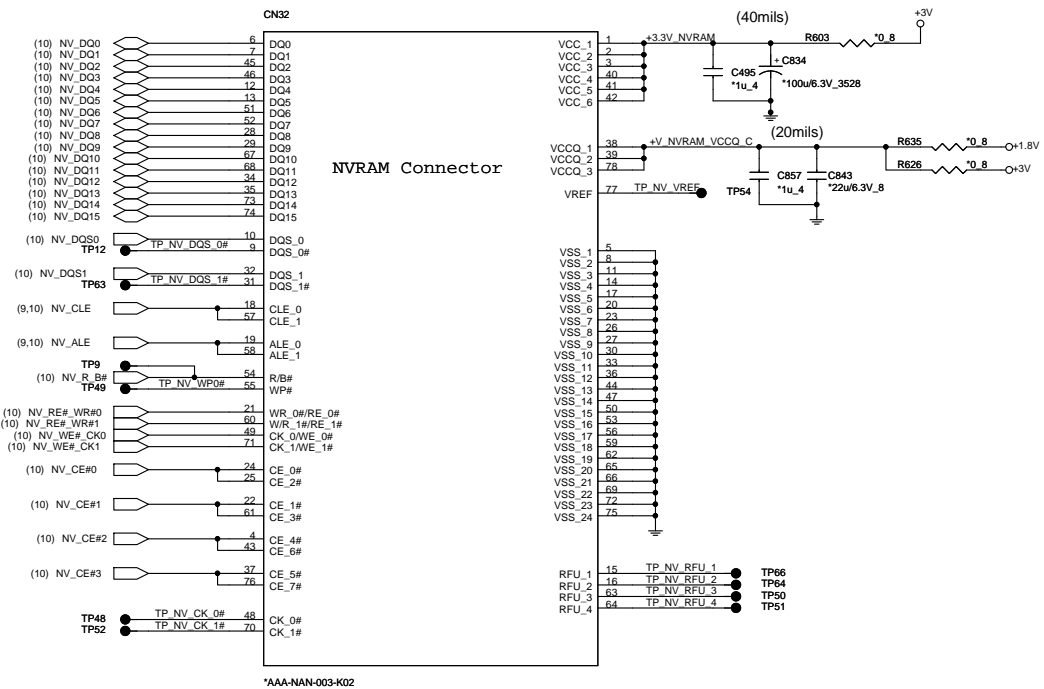
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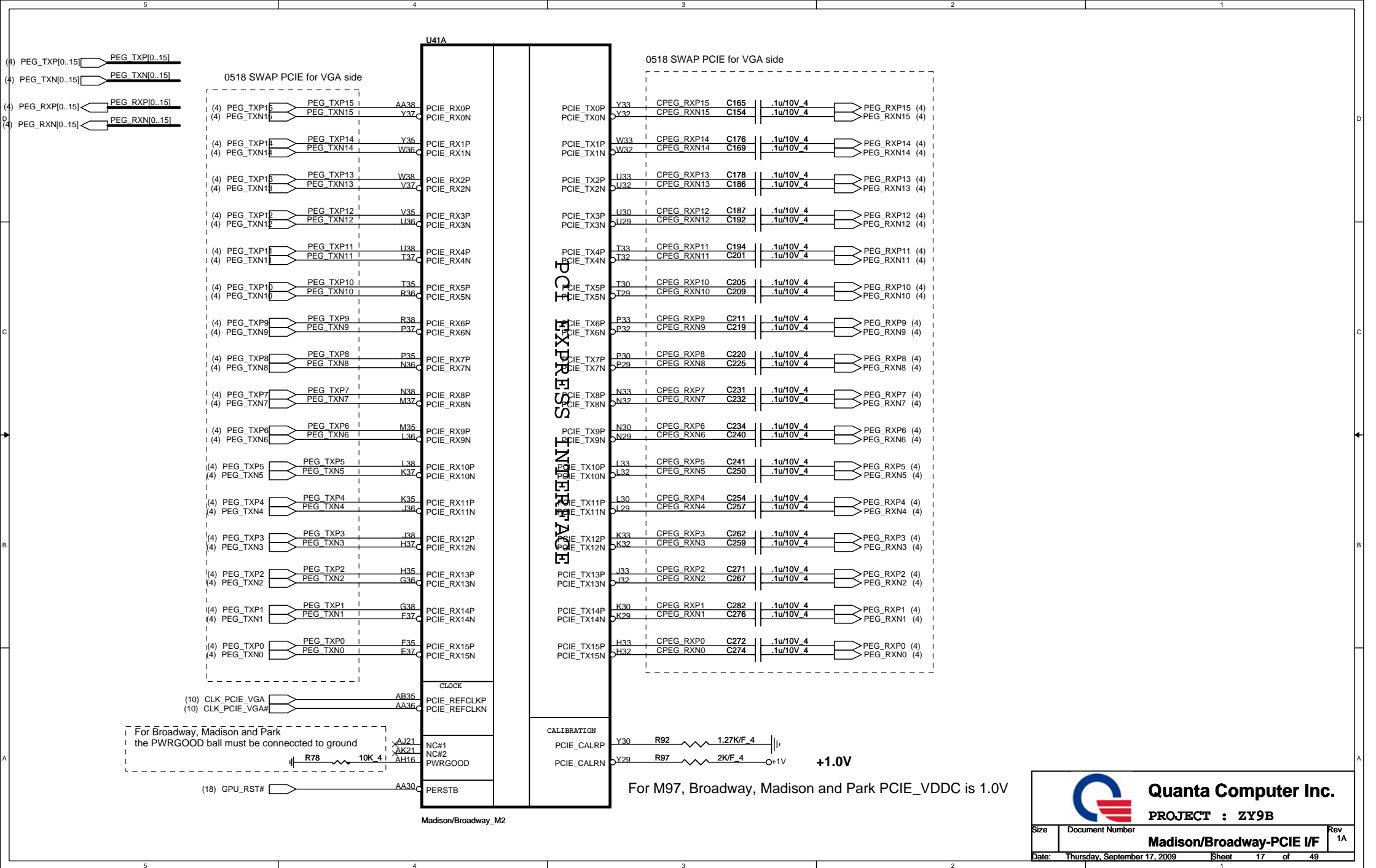
PROJECT : ZY9B

CPU XDP Connector

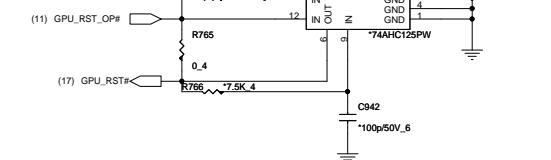
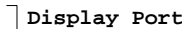
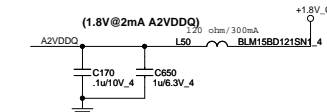
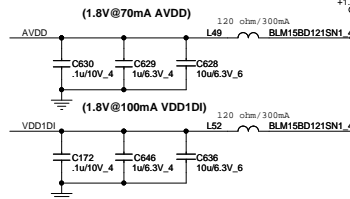
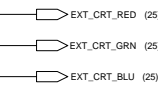
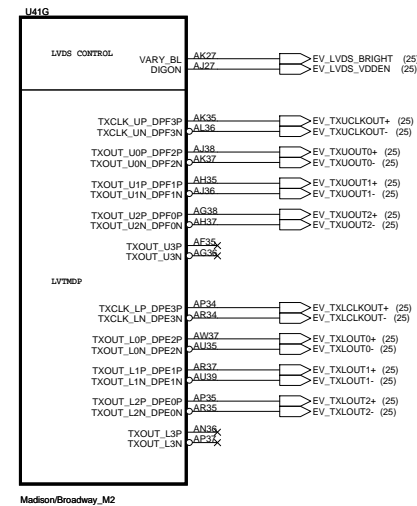
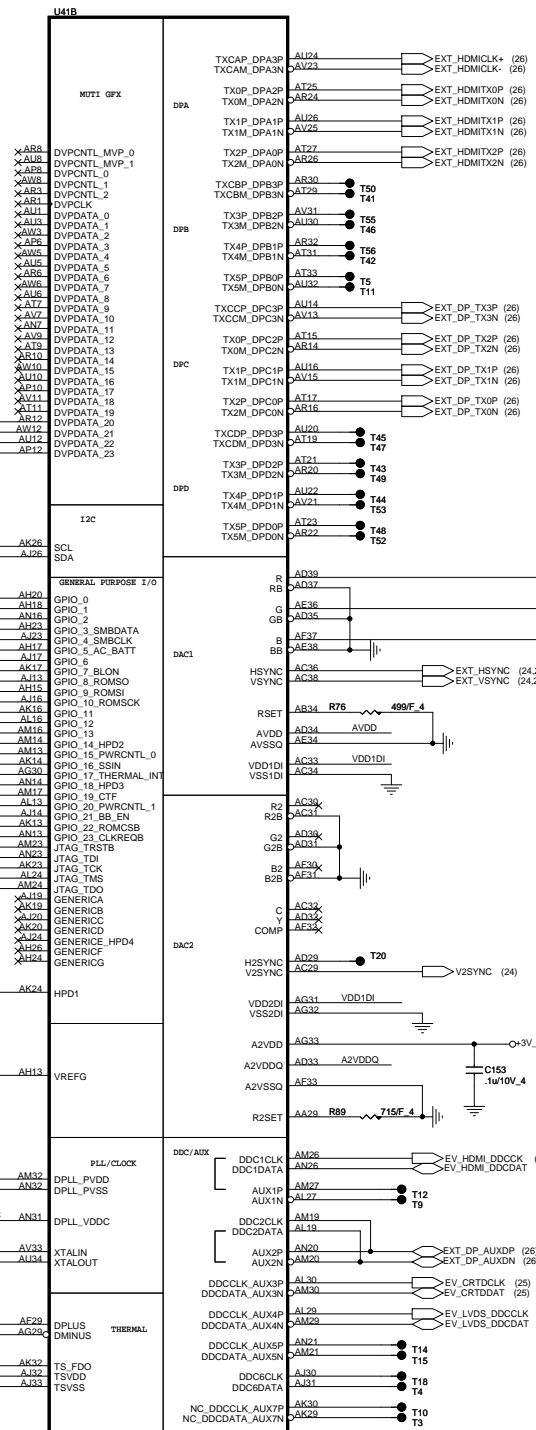
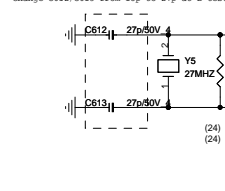
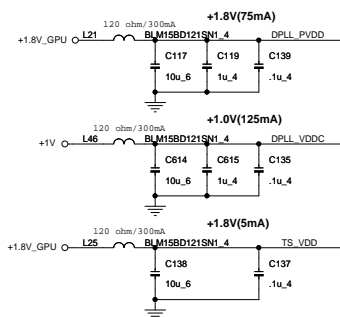


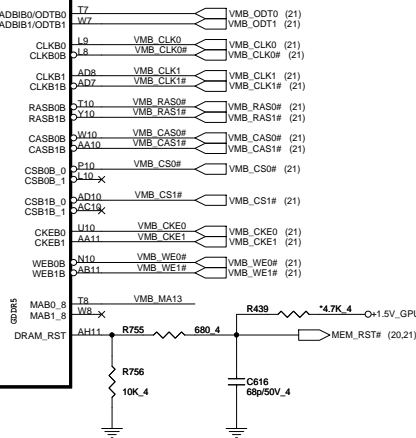
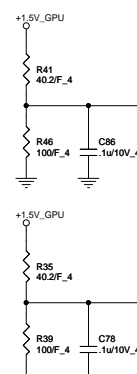
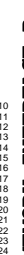
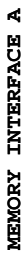
Braidwood





```
1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK
```

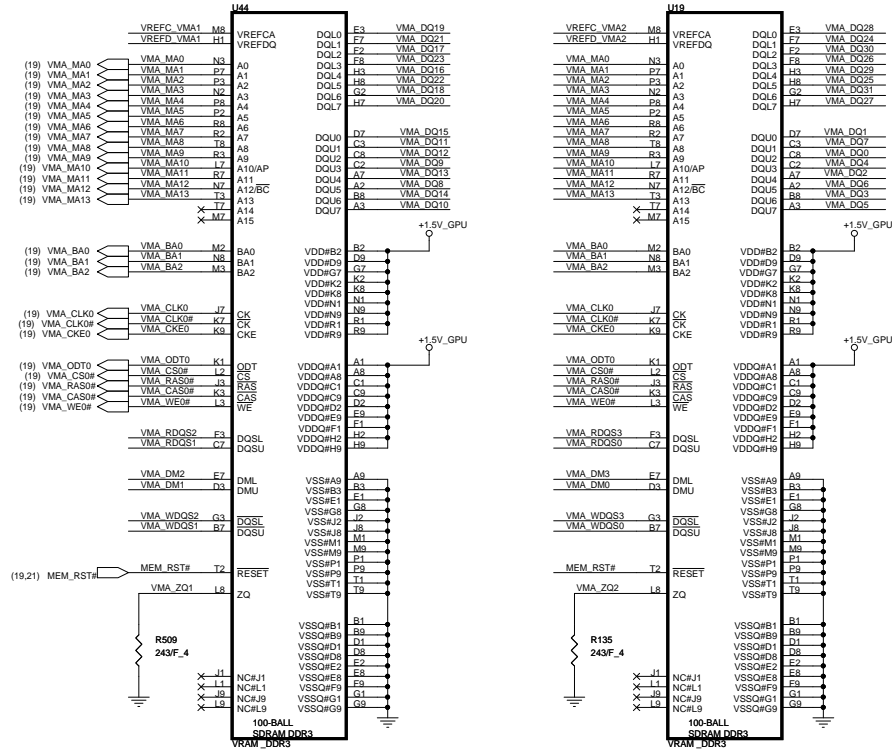




CHANNEL A: 512MB DDR3 (64M*16*4pcs)

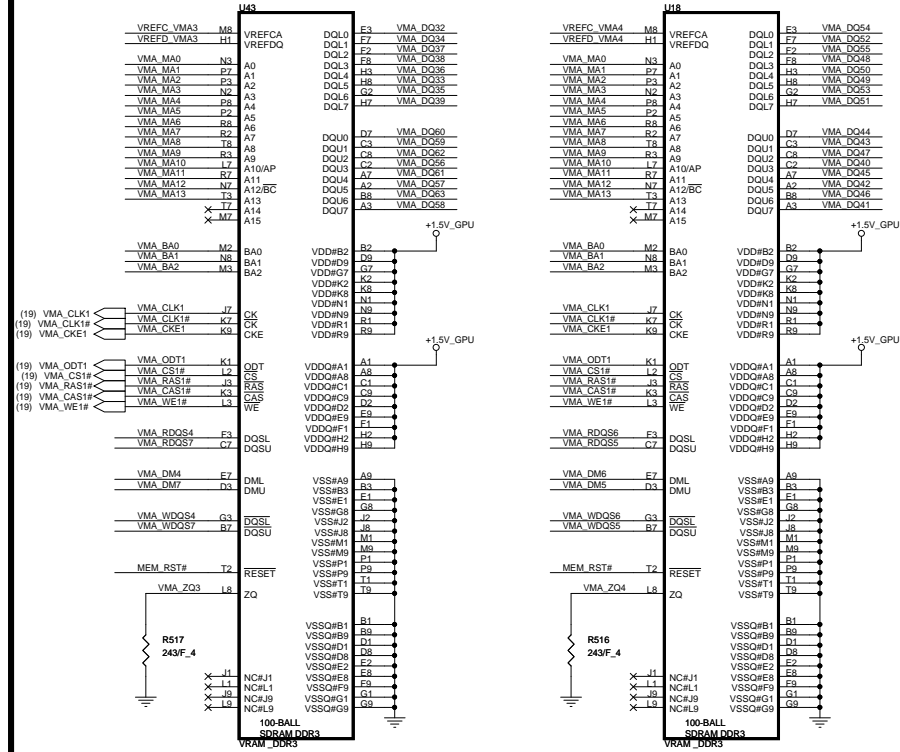
(19) VMA_DQ[63..0] VMA_DQ[63..0]
 (19) VMA_DM[7..0] VMA_DM[7..0]
 (19) VMA_RDQS[7..0] VMA_RDQS[7..0]
 (19) VMA_WDQS[7..0] VMA_WDQS[7..0]

QSA[7..0]
 QSA[7..0]



TOP Left

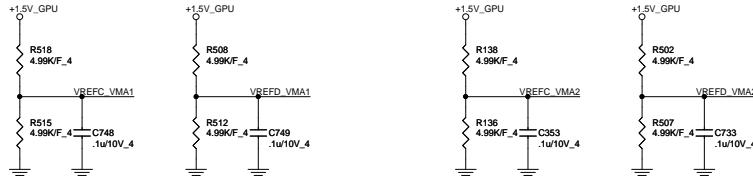
BOT Left



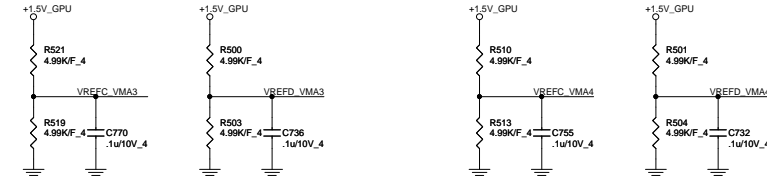
BOT Right

TOP Right

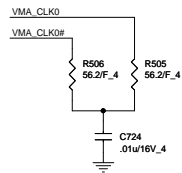
Group-A0 VREF



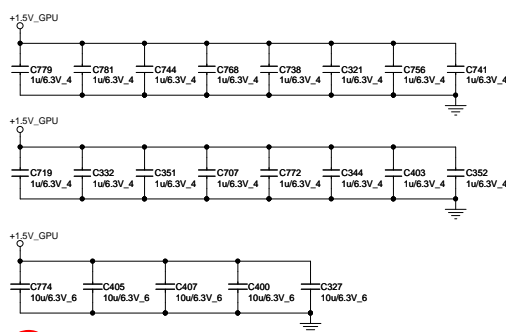
Group-A1 VREF



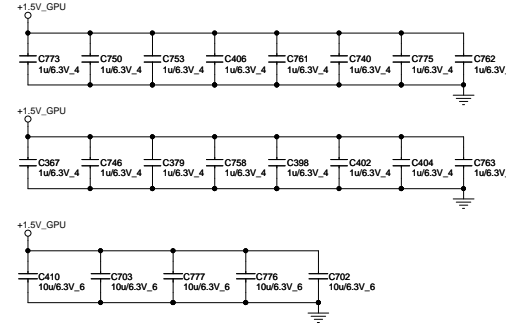
MEM_A0 CLK



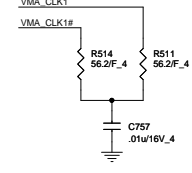
Group-A0 decoupling CAP



Group-A1 decoupling CAP



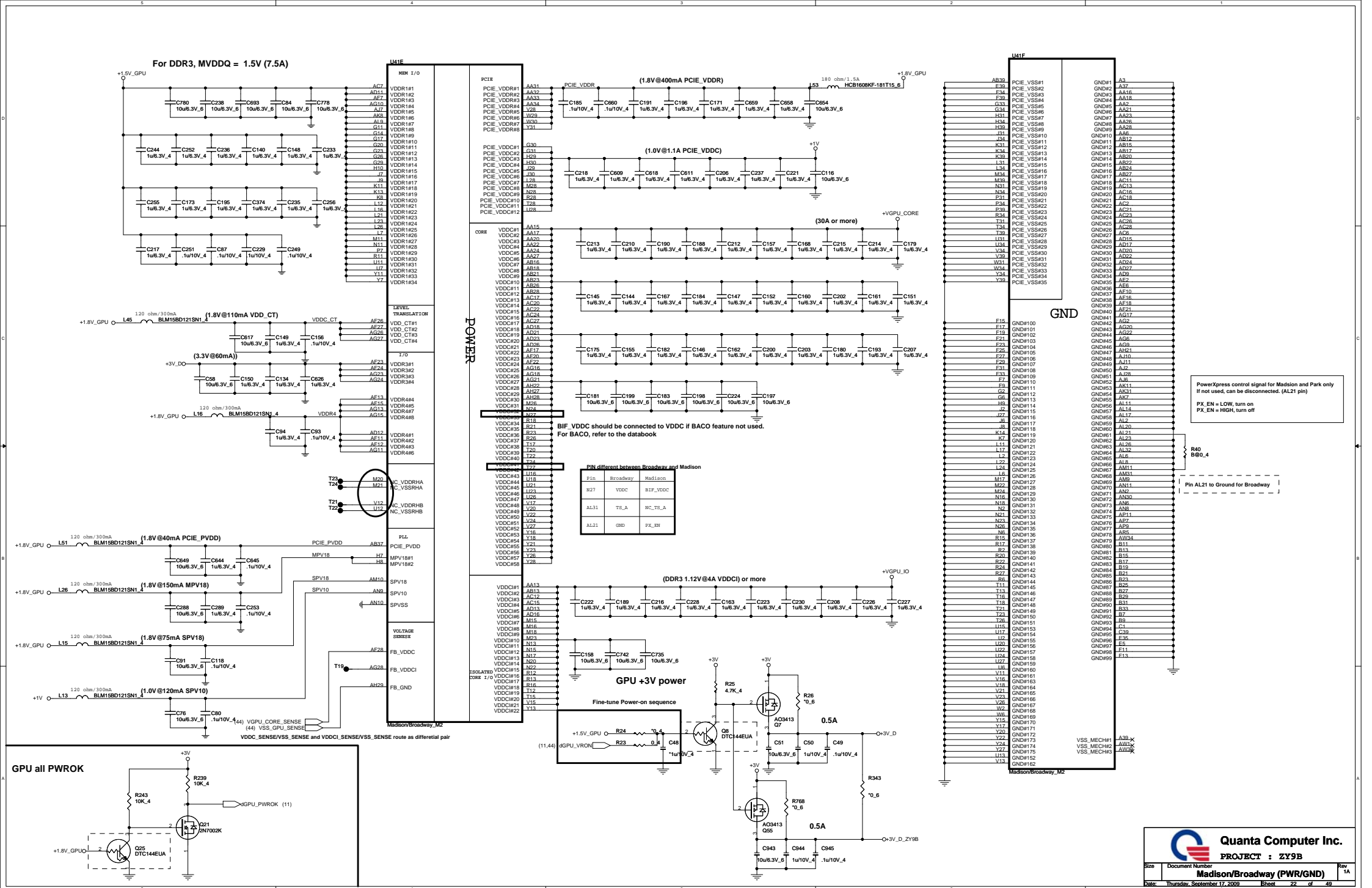
MEM_A1 CLK



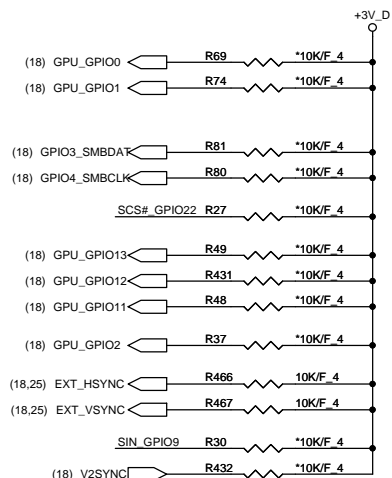
Quanta Computer Inc.
 PROJECT : ZY9B

Size Document Number
 Date: Thursday, September 17, 2009 Sheet 20 of 49

[illegible]



PIN STRAPS



Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Audio Table

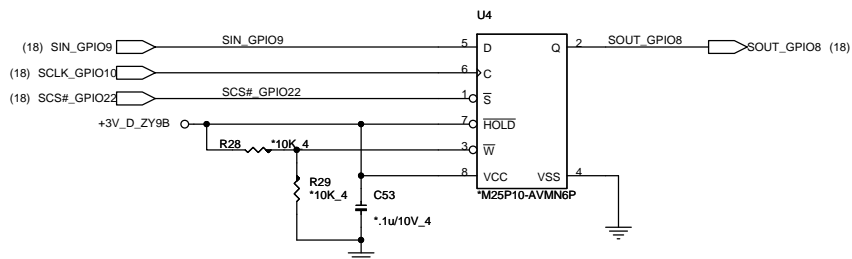
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM

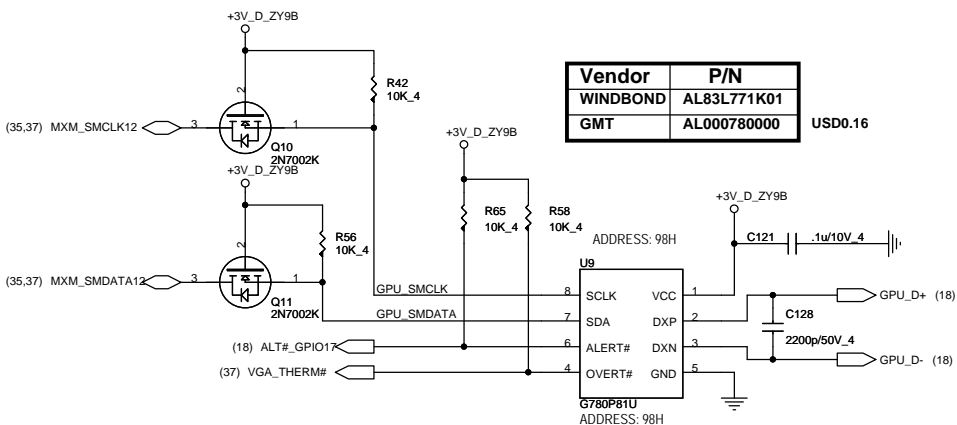


DDR3 VRAM SIZE Strap

DDR3 VRAM size

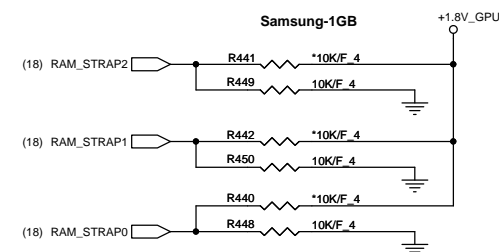
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB			
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB	0	1	0
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1

Thermal Sensor



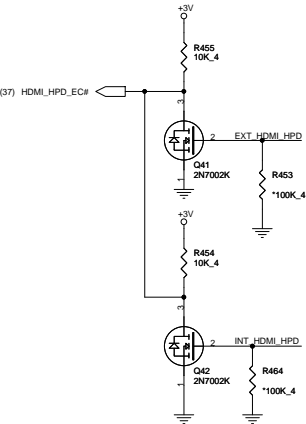
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16

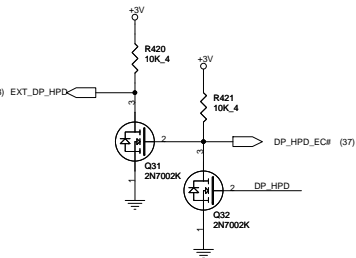


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

HDMI Hot-PLUG to EC and GPU



DP Hot-PLUG to EC and GPU



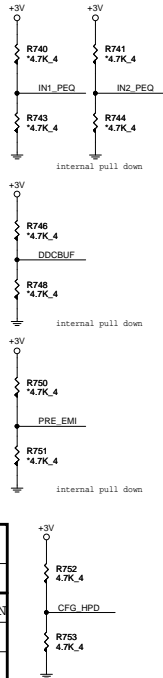
HDMI

Input EQ setting	
INn_PEQ	Output
L	Middle EQ
H	High EQ
M	Low EQ

DDC Buffer setting	
DDC_BUF	Output
L	Passive DDC
H	Active Set-1
M	Active Set-2

Pre-emphasis and EMI setting	
PRE_EMI	Output
L	No_PRE&EMI
H	PRE enable
M	EMI control

Hot-plug detect	
CFG_HPD	Output
L	Follow SW_MAIN
H	Follow SW_DDC
M	SW or DDC

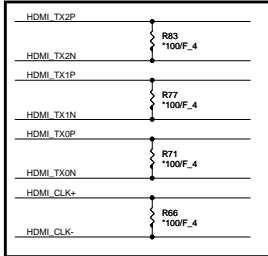


From EXT VGA

From INT

SW	Yn	Output
0	dGPU	Port-1
1	UMA	Port-2

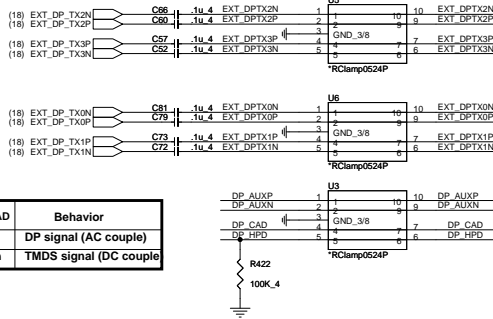
EMI reserve for HDMI



close CN24

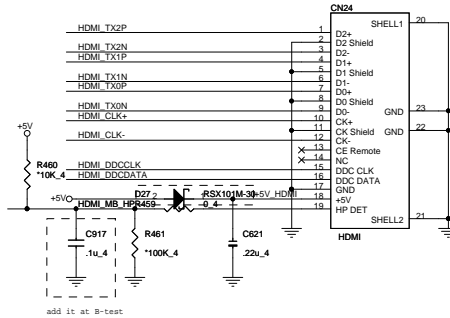
ESD Protect

close to DP connector

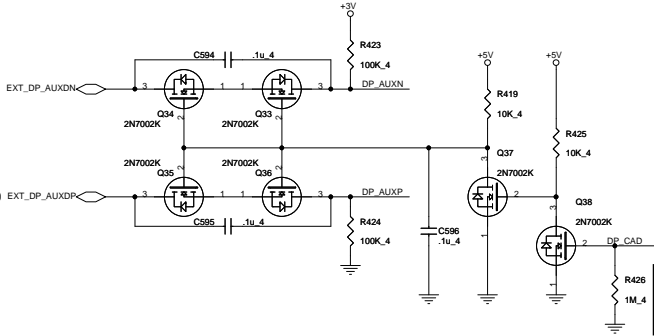


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

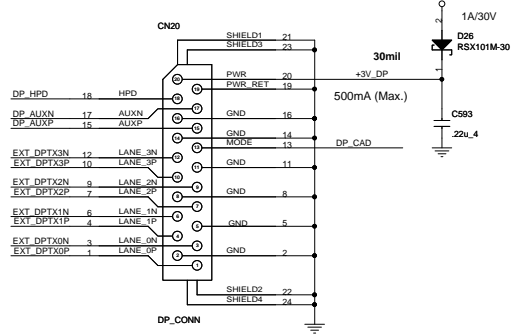
HDMI connector



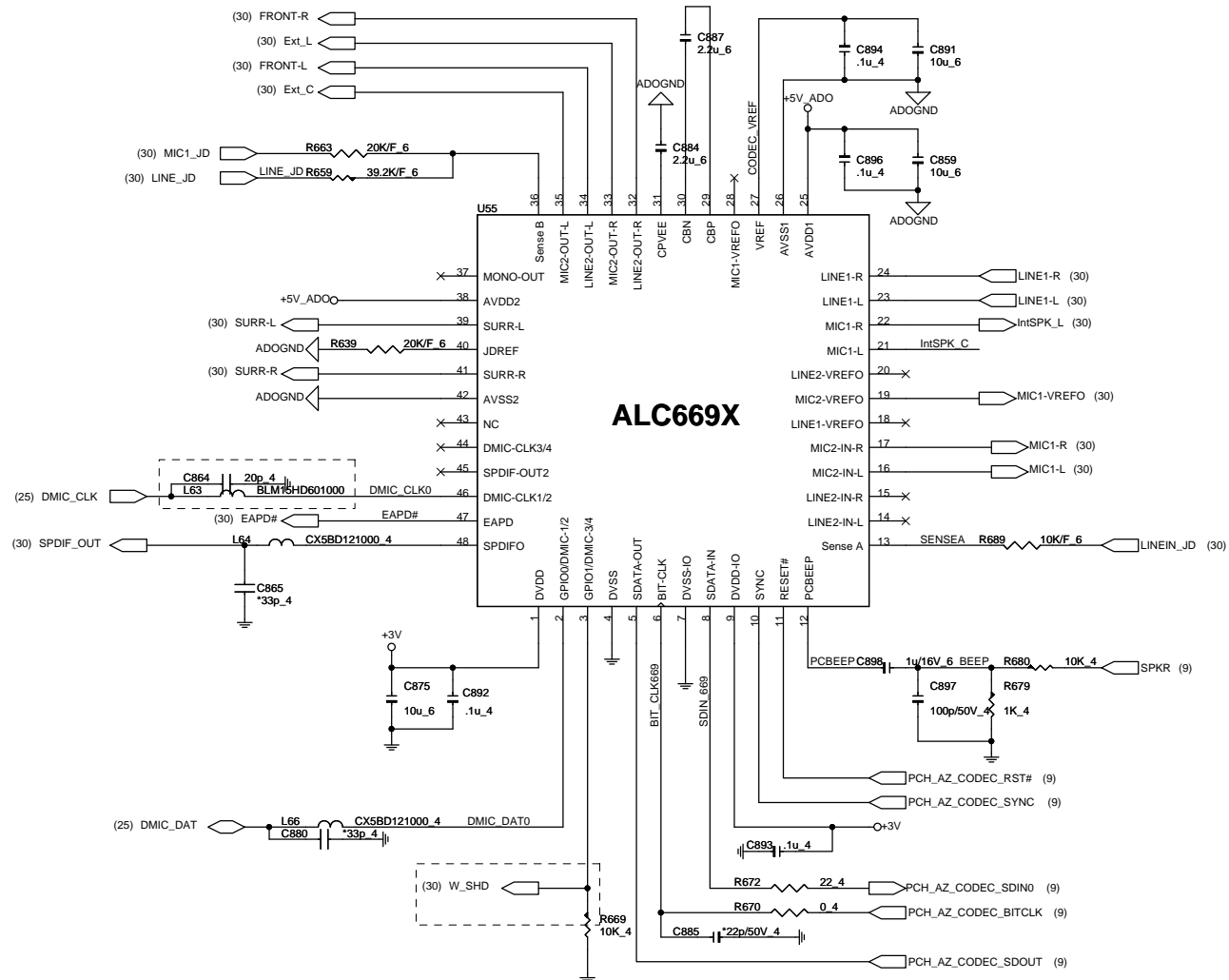
DisplayPort



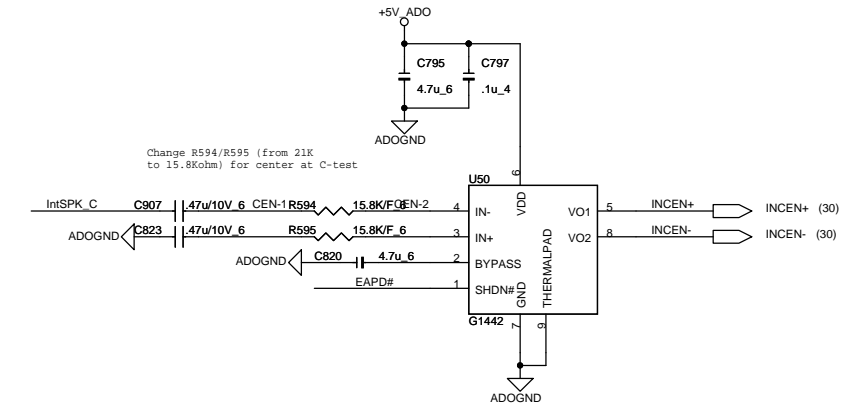
DP connector



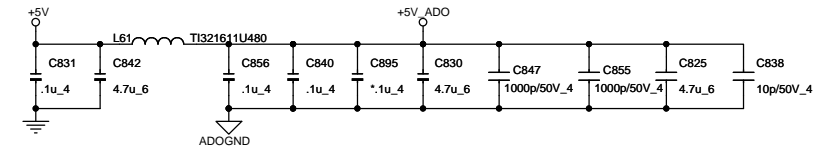
CODEC(ALC669X)




CENTER MONO



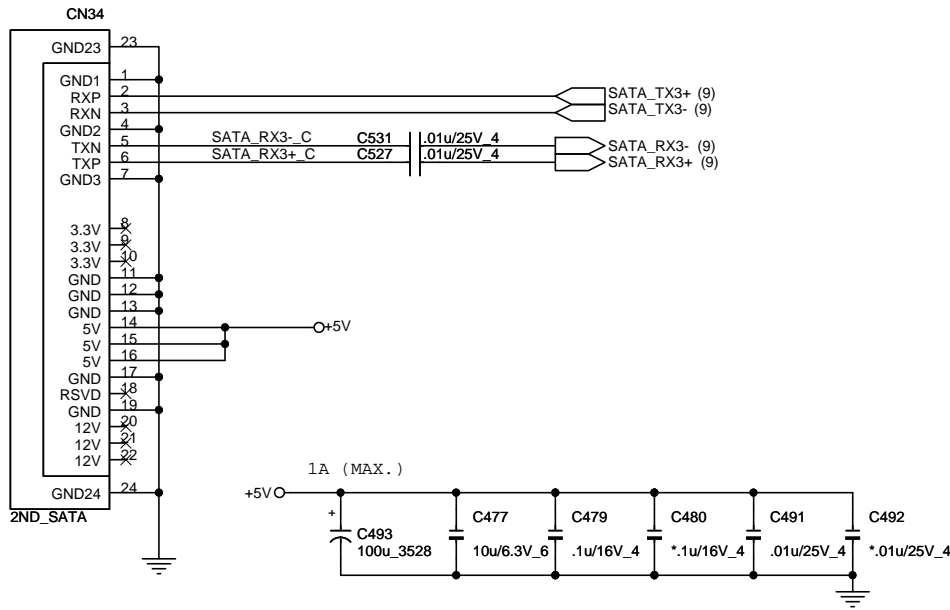
CODEC/AMP Power



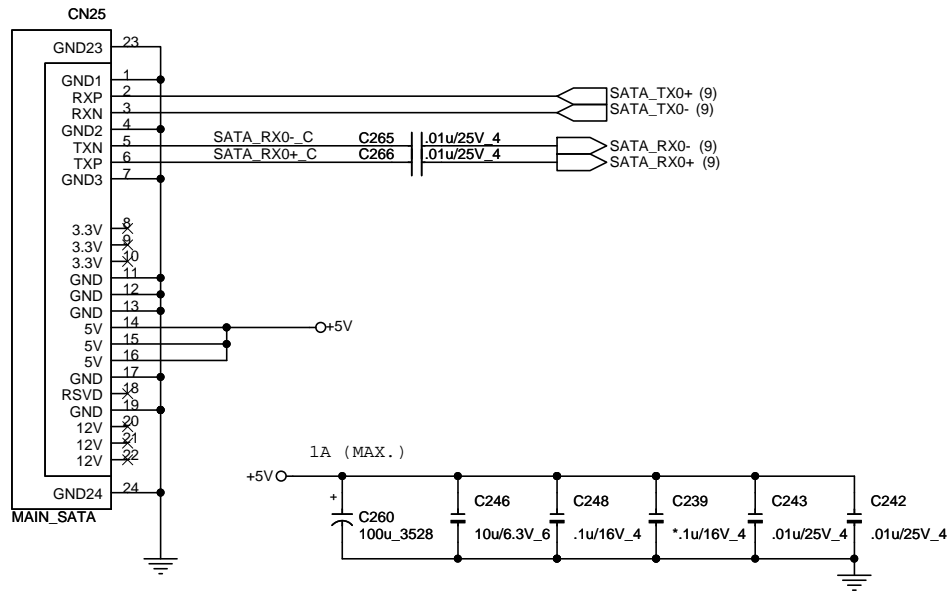

Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev 1A
REALTEK ALC889X/MONO-AMP		
Date:	Thursday, September 17, 2009	Sheet 29 of 49

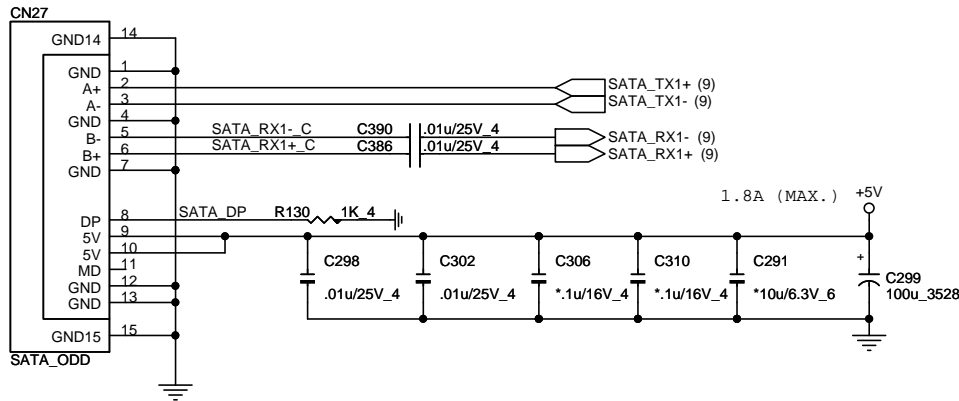
2nd SATA HDD (edge of board)



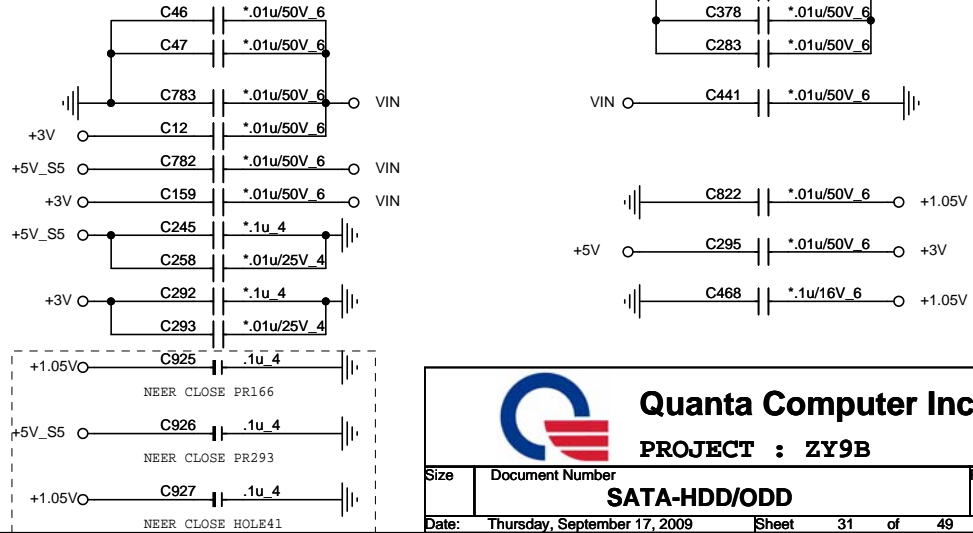
MAIN SATA HDD




ODD (SATA)



EE RETURN-PATH CAPACITORS





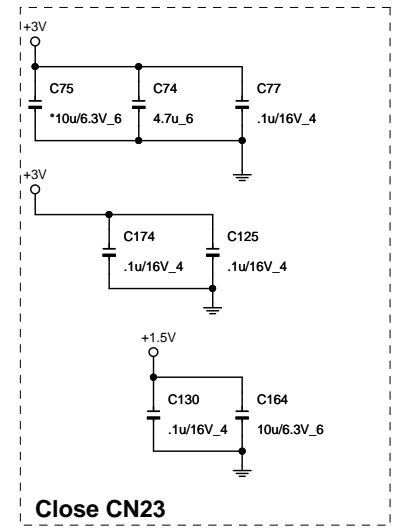
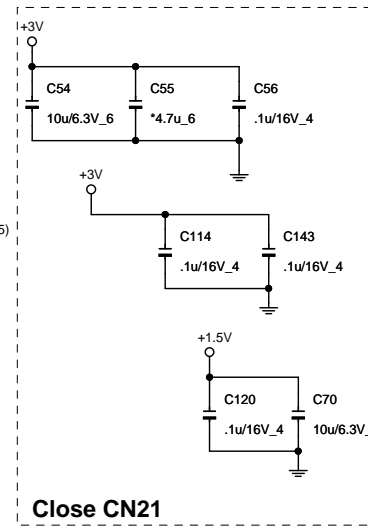
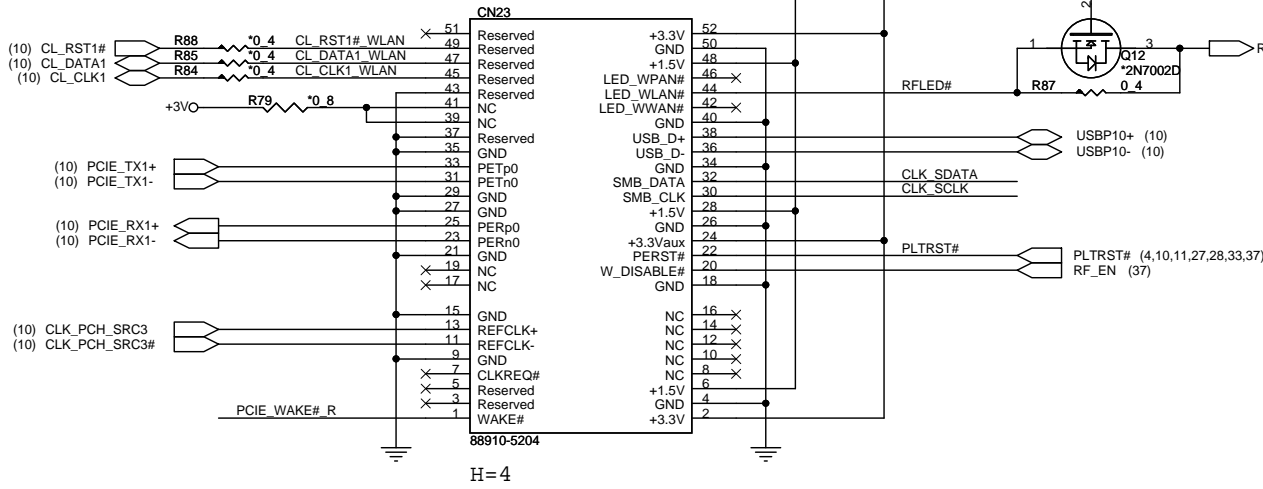
Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date:	Thursday, September 17, 2009	Sheet 31 of 49

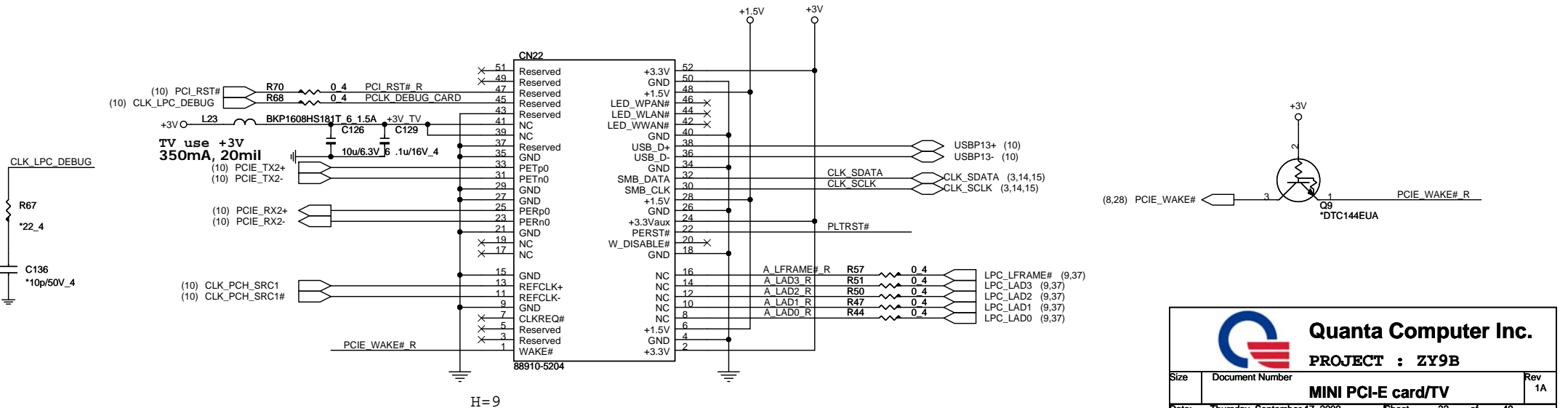
Wireless

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



TV and Debug



Quanta Computer Inc.

PROJECT : ZY9B

Size: Document Number

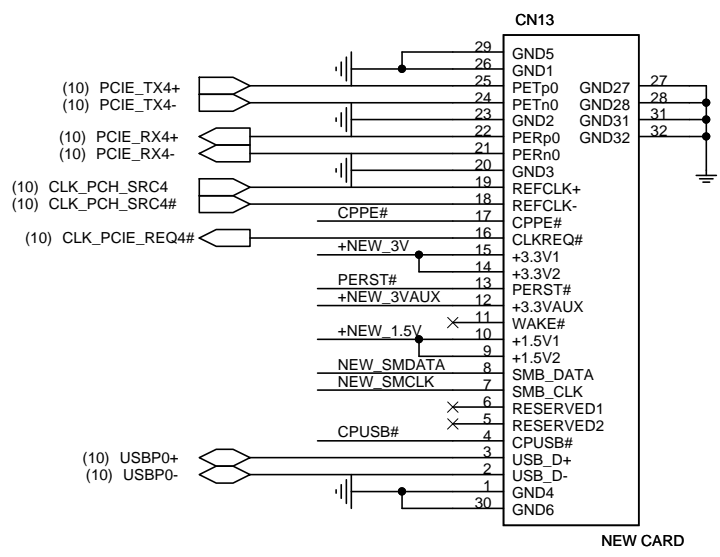
Date: Thursday, September 17, 2009

MINI PCI-E card/TV

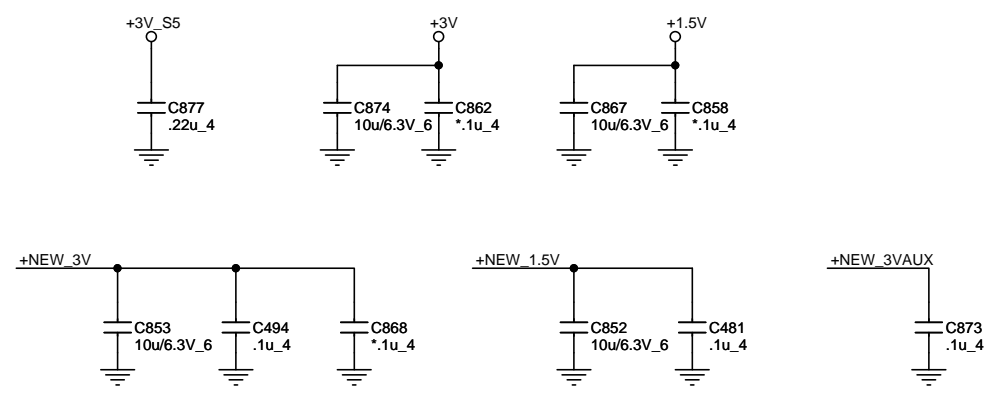
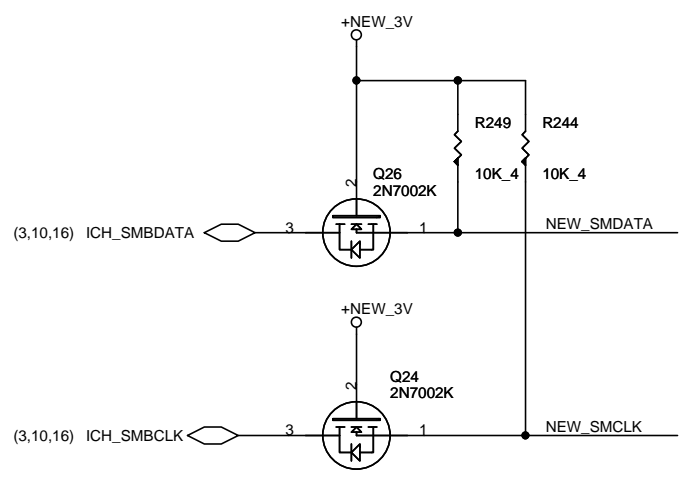
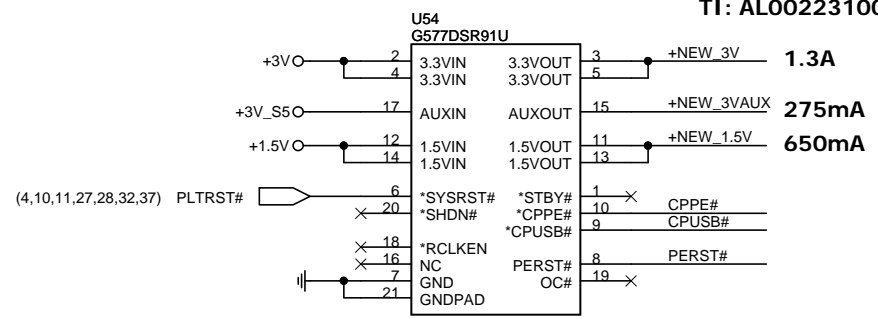
Sheet 32 of 49


Rev 1A

NEW CARD



NEW CARD'S POWER SWITCH GMT: AL000577002
TI: AL002231000

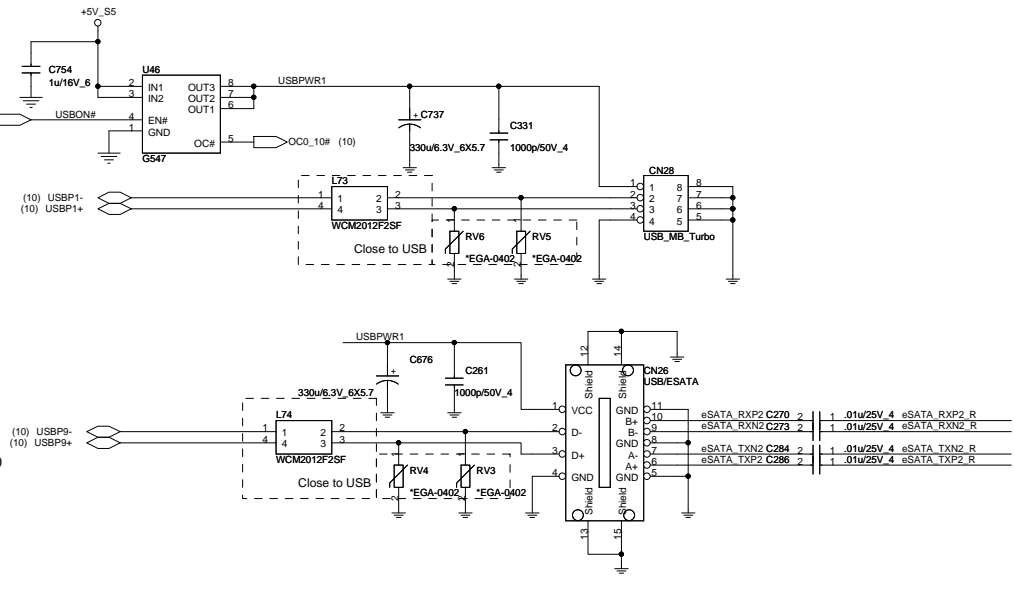
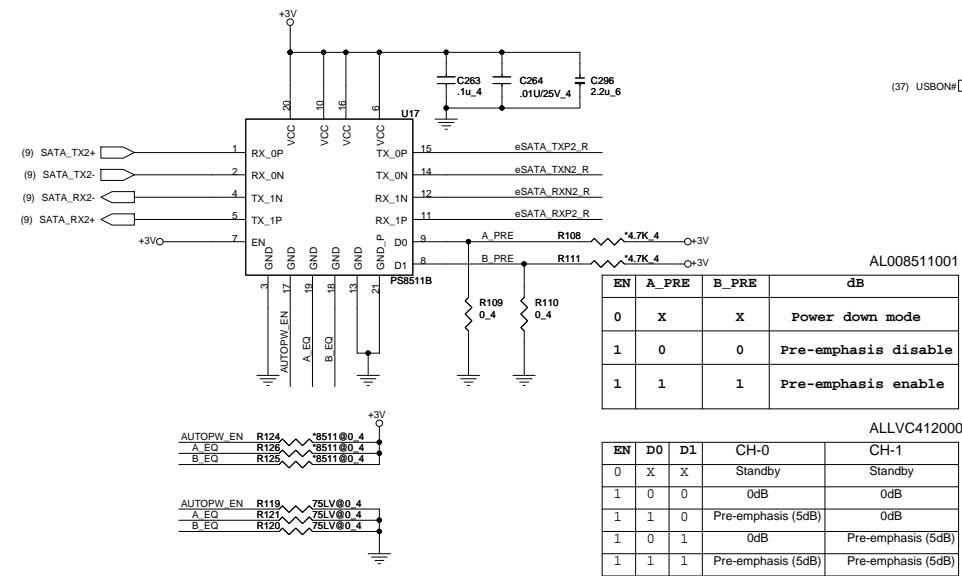




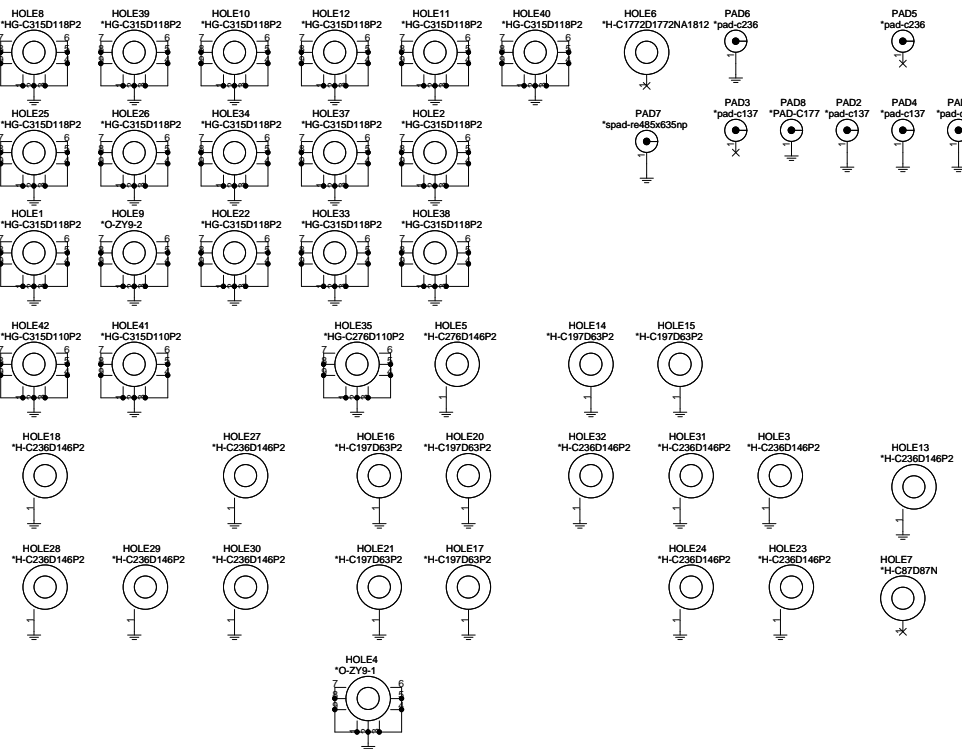
Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev 1A
NEW CARD		
Date: Thursday, September 17, 2009	Sheet 33 of 49	

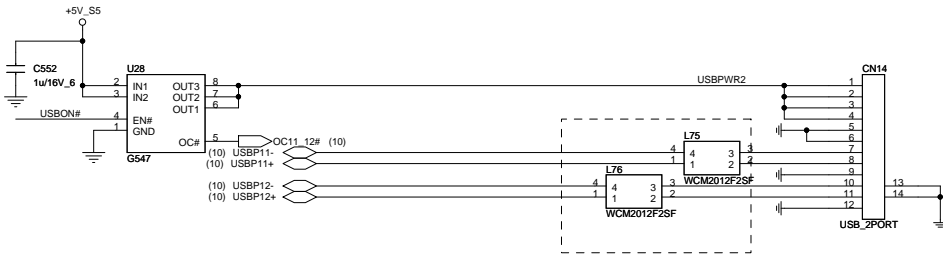
USB & ESATA



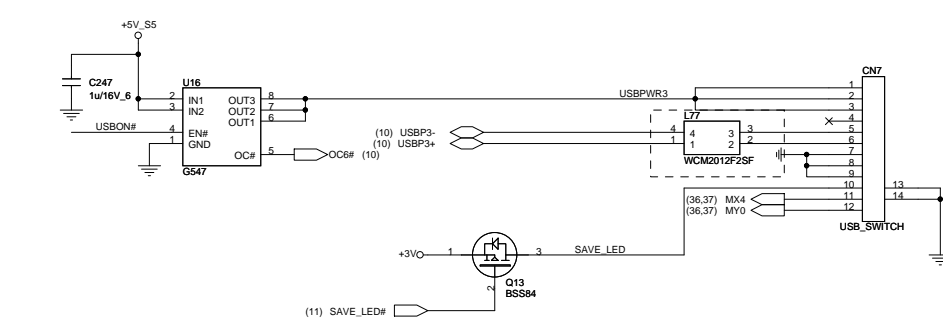
HOLES



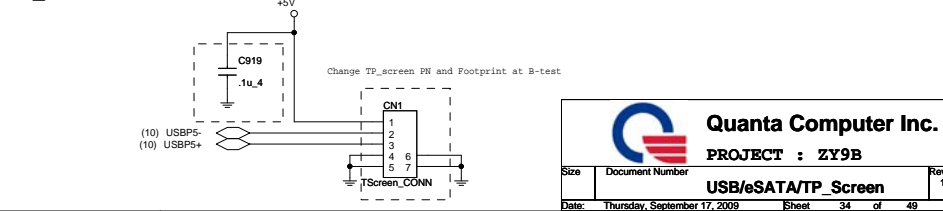
USB_2PORT/B



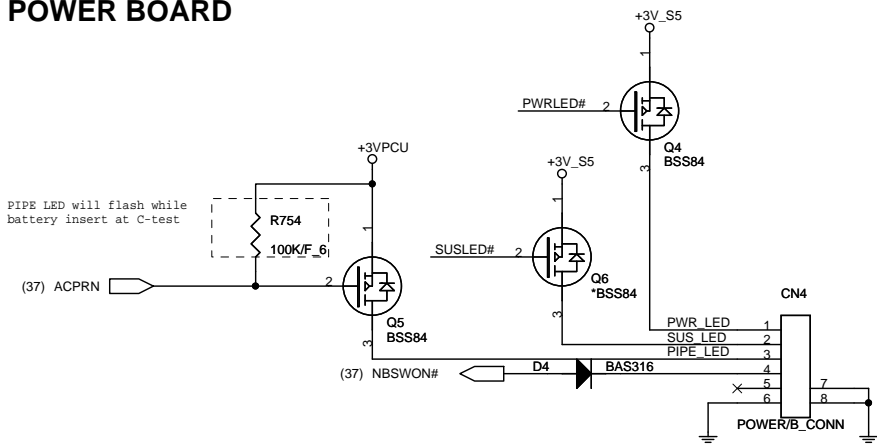
USB_SWITCH/B



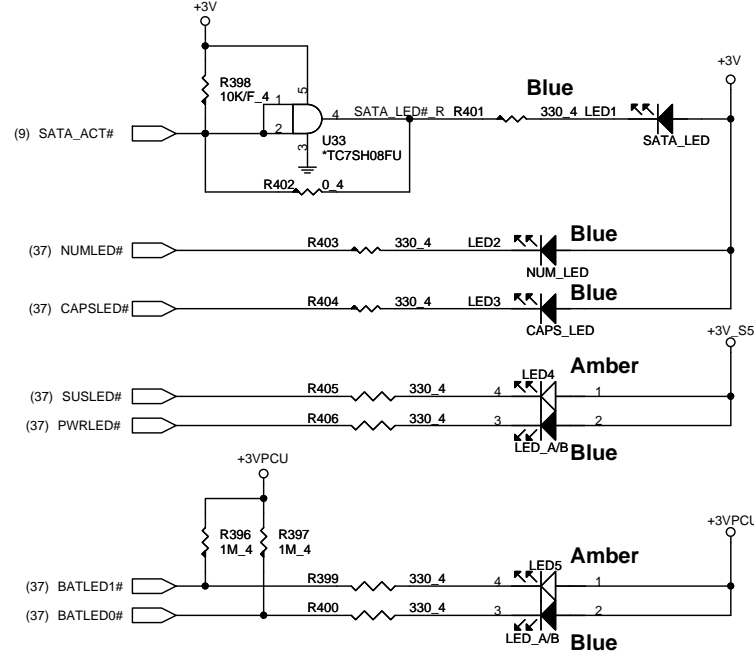
TP_Screen



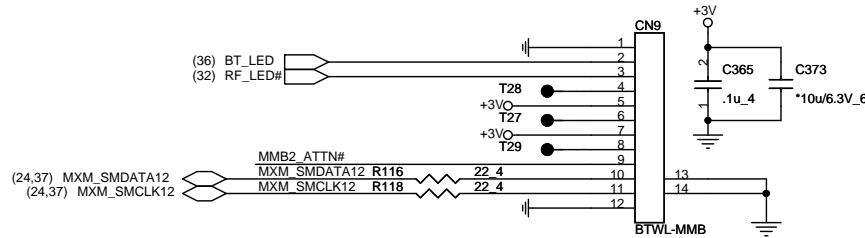
POWER BOARD



M/B LED

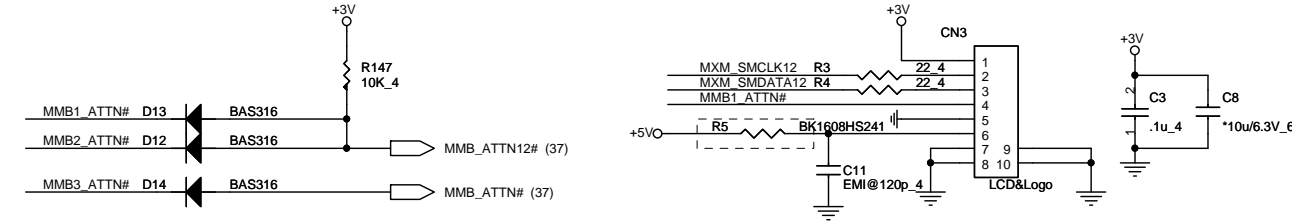


Left side MMB

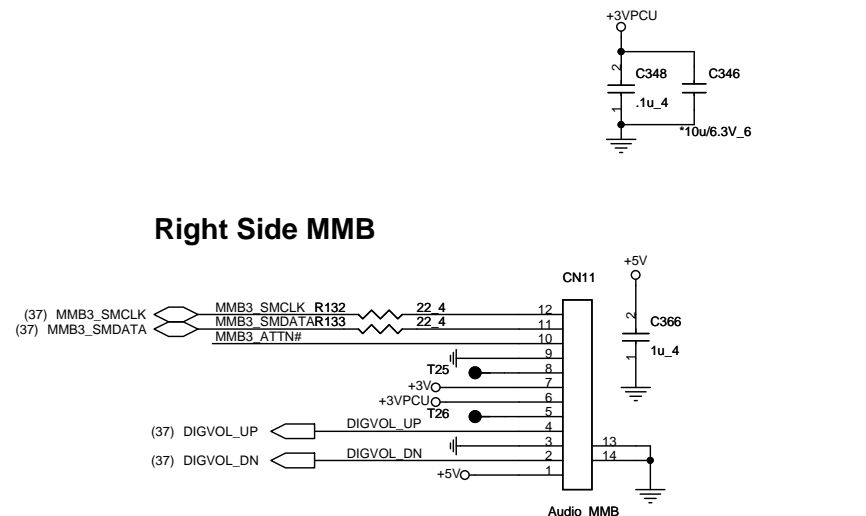



MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.
LCD BL_ON/OFF MMB & Backlight Logo LED

MMB Status



Right Side MMB

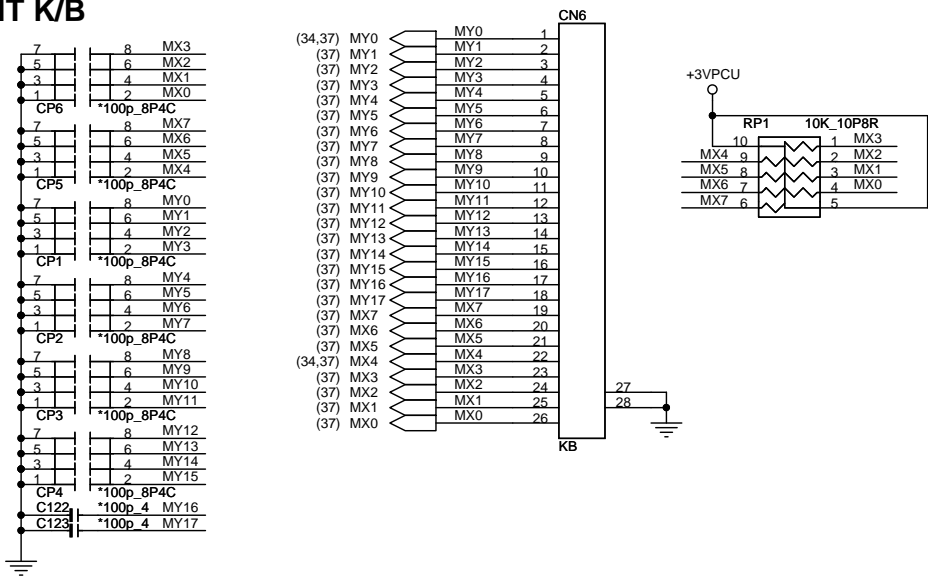




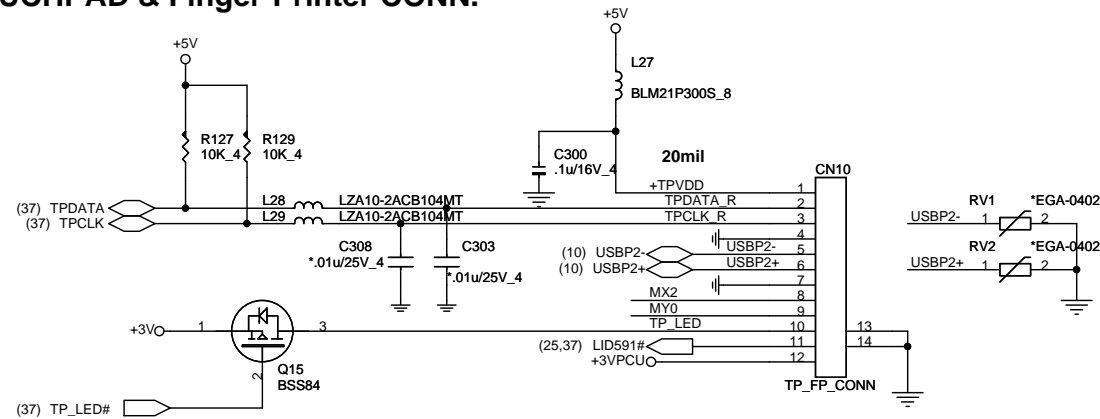
Quanta Computer Inc.
PROJECT : ZY9B
POWER/MMB/LAUNCH/LED

Size	Document Number	Rev 1A
Date: Thursday, September 17, 2009		Sheet 35 of 49

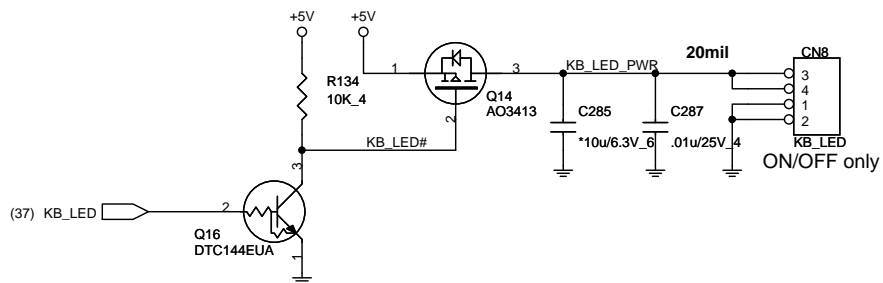
INT K/B



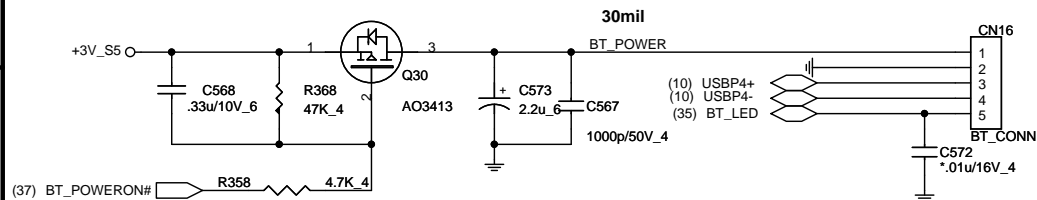
TOUCHPAD & Finger-Printer CONN.



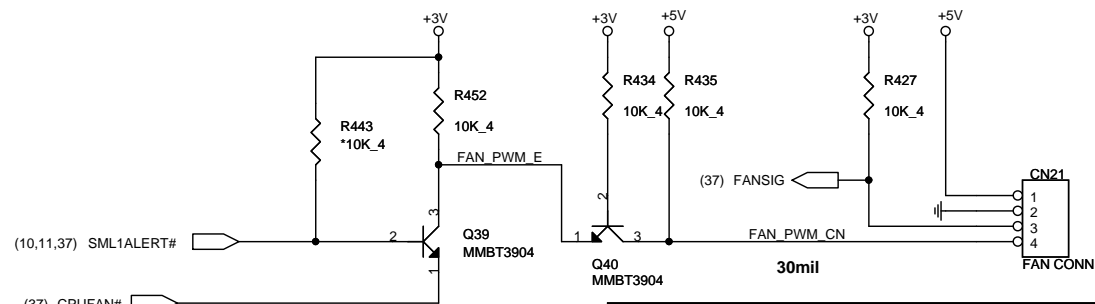
Keyboard LED control



BLUETOOTH CONNECTOR



CPU FAN

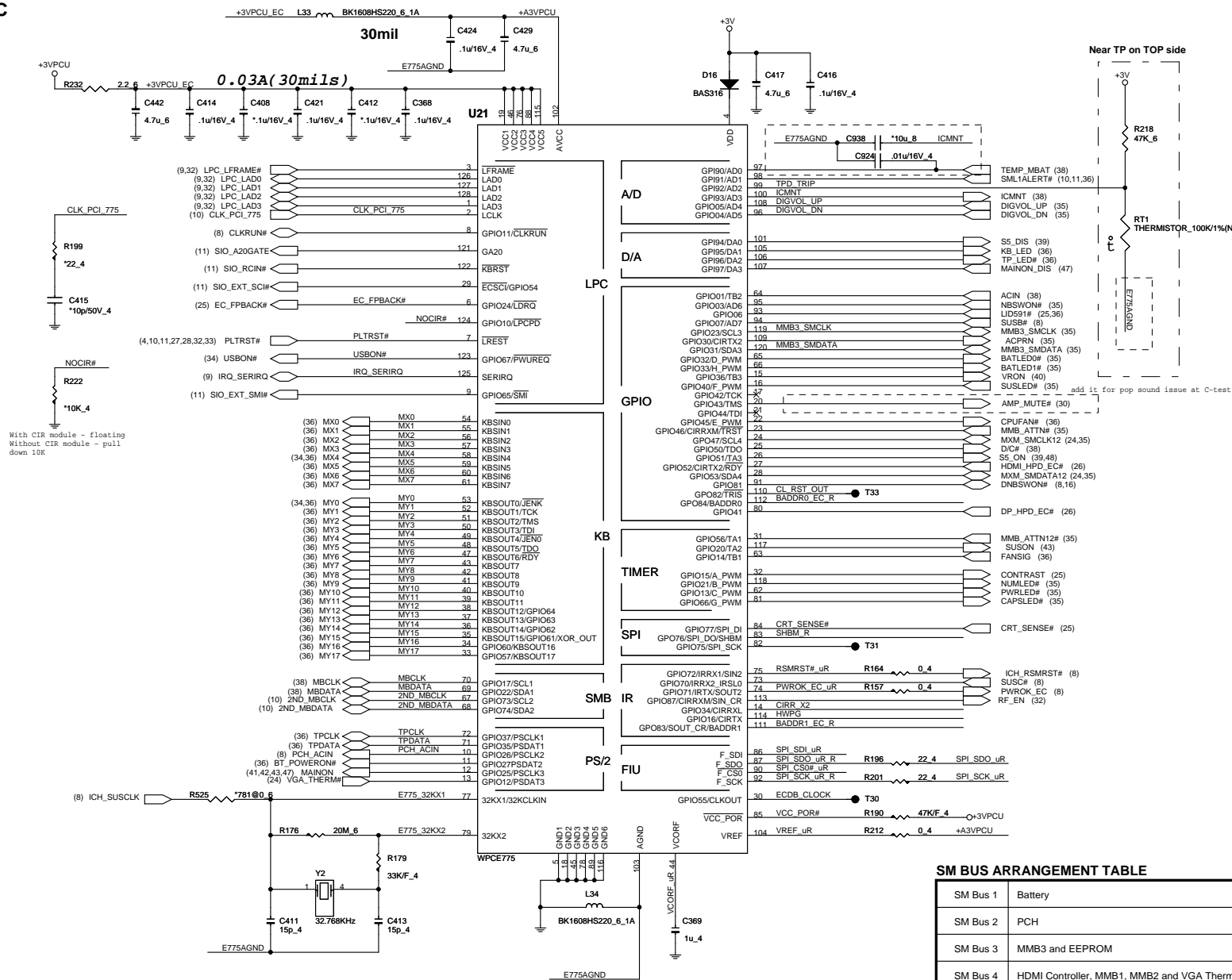


Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	KB/FAN/TP+FP/BT	1A

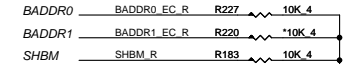
Date: Tuesday, September 22, 2009 Sheet 36 of 49



I/O ADDRESS SETTING

I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

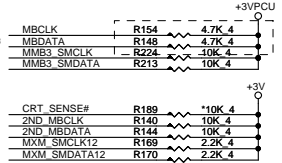
SHBM=0: Enable shared memory with host BIOS



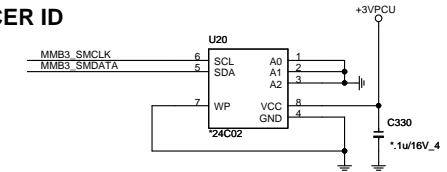
1/13 Confirm by vendor mail :
 Disabled (*) if using FWH device on LPC.
 Enabled (0) if using SPI flash for both system BIOS and EC firmware

SM BUS PU

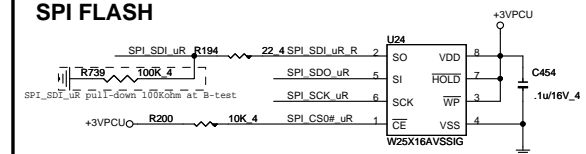
Change pull-up resistor (R148, R154) from 10K to 4.7Kohm



ACER ID



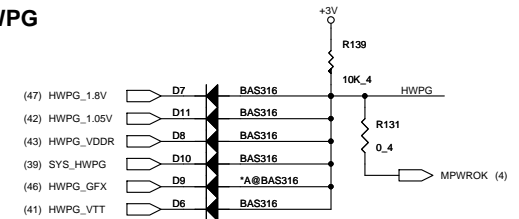
SPI FLASH



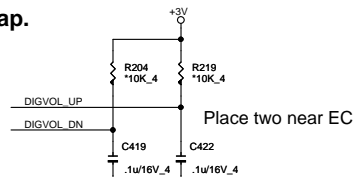
1/13 Confirm by vendor mail :
 If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add:
 Winbond W25X16AVSSIG
 MXIC MX25L1605AM2C-15G
 EON EN25F16-100HIP
 AMIC A25L016
 AKE38ZPN01
 AKE37FP0213
 AKE38ZAO000
 AKE38ZNO800

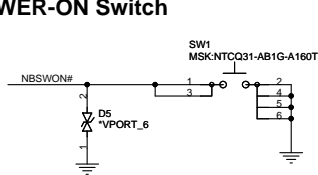
HWPG



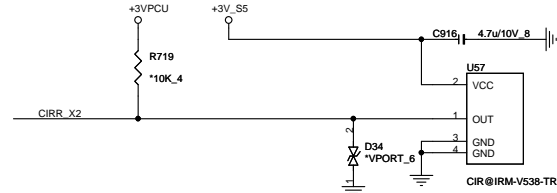
VR Cap.



POWER-ON Switch



CIR



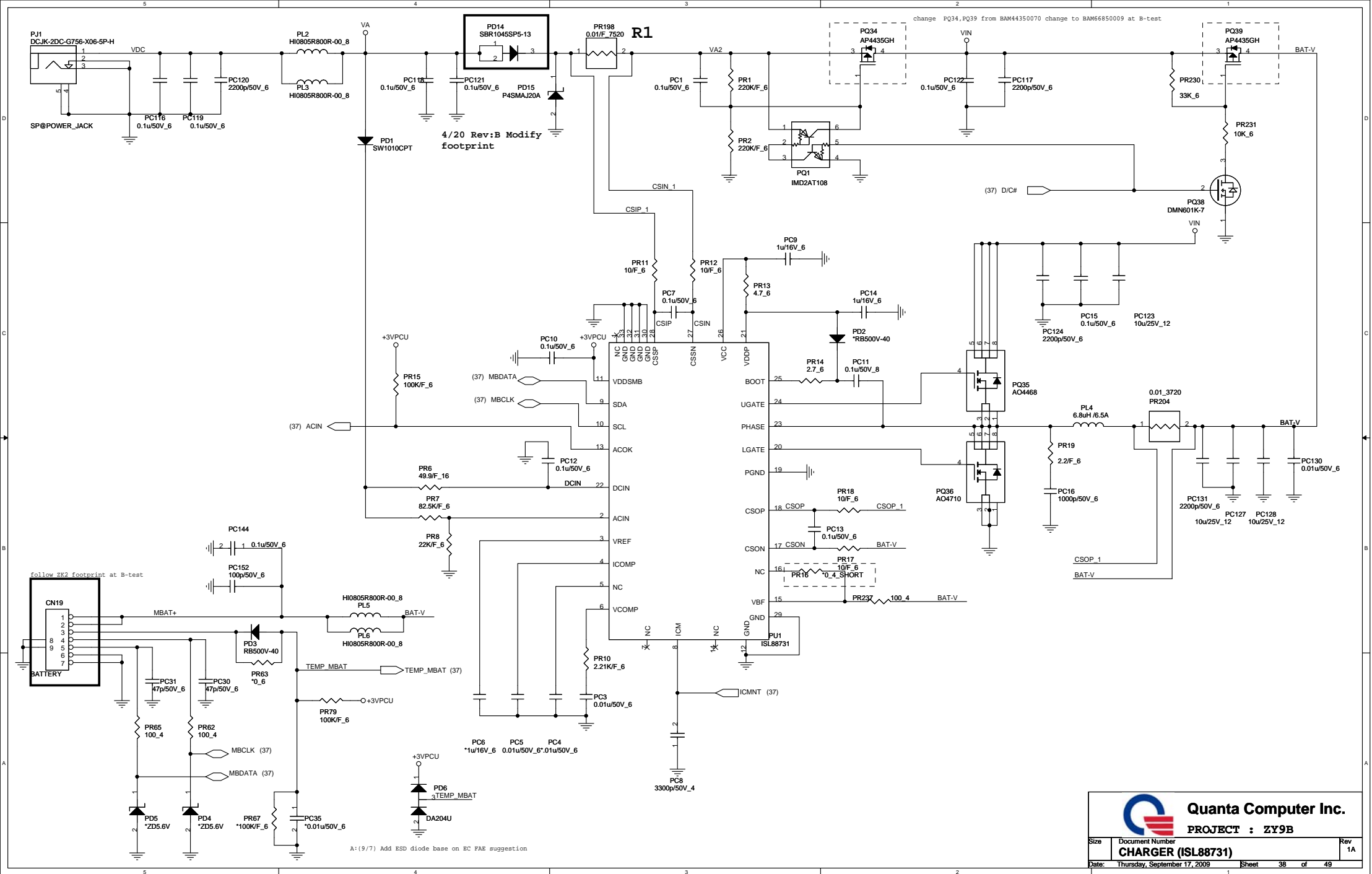
INTERNAL KEYBOARD STRIP SET

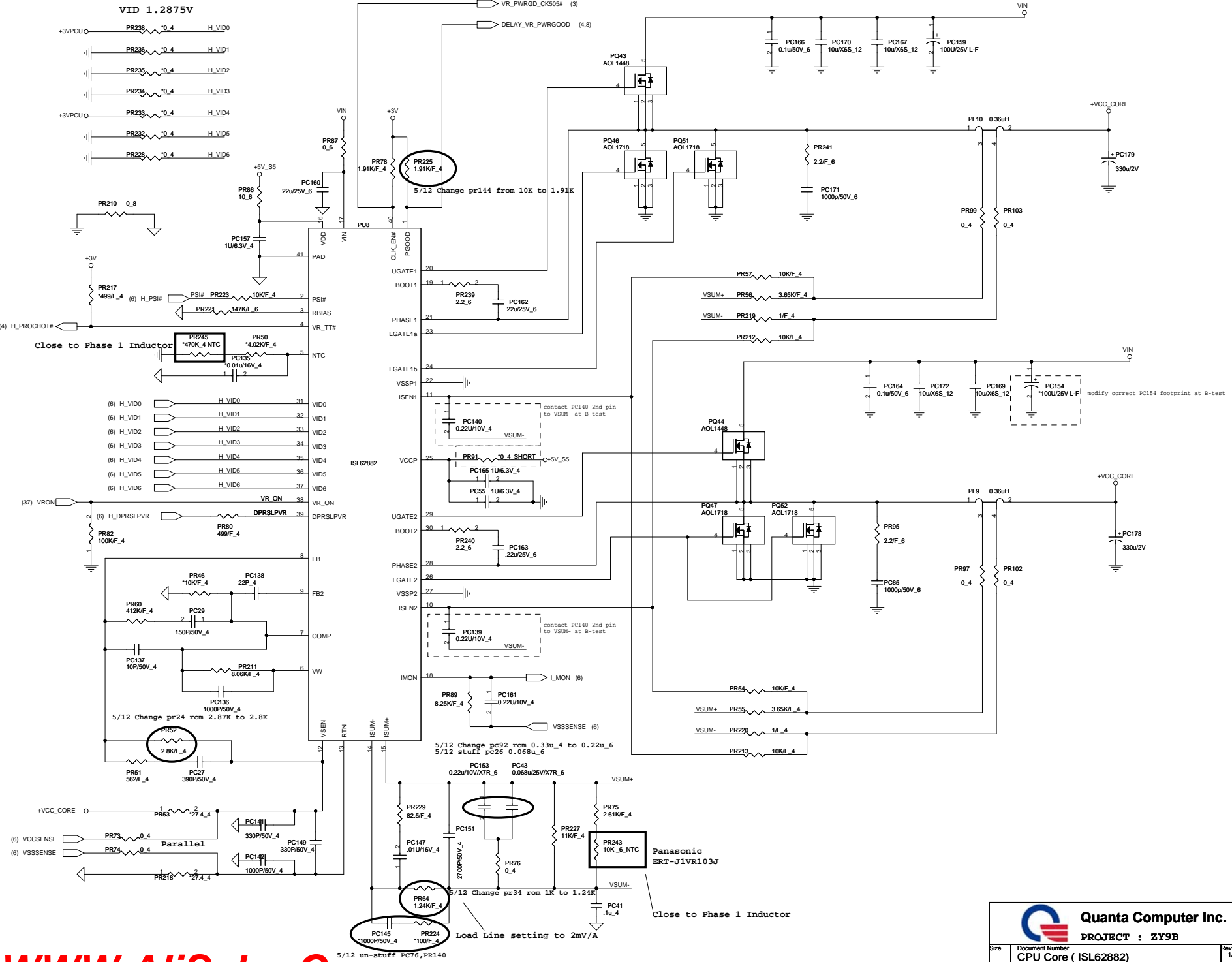


Quanta Computer Inc.

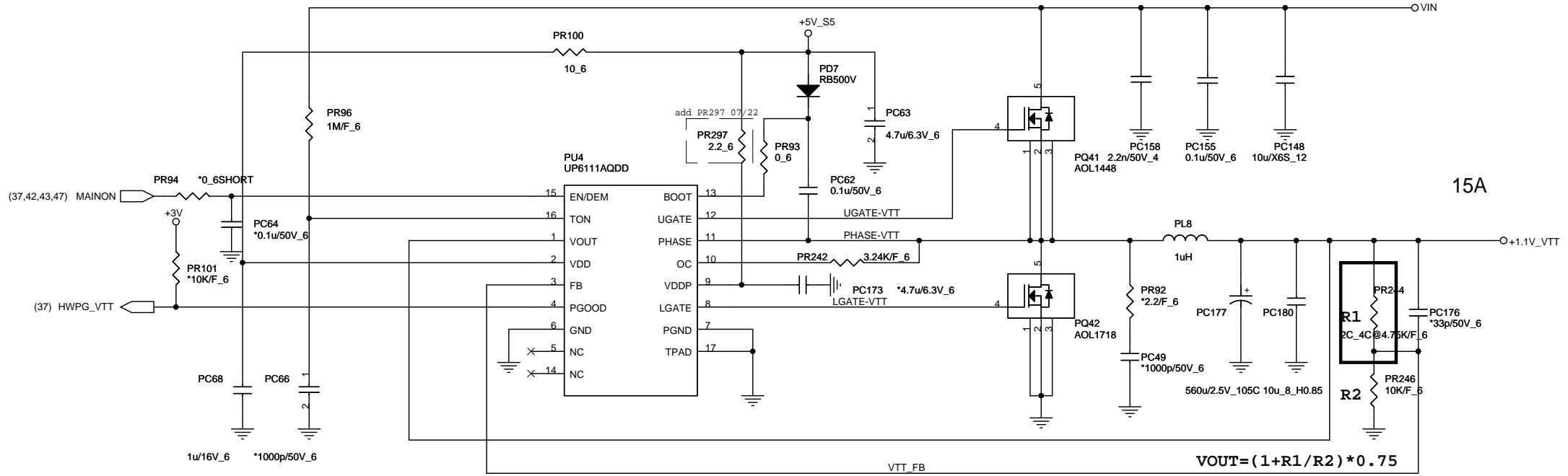
PROJECT : ZY9B

Size	Document Number	Rev
	WPCE775C_ODG & FLASH	1A
Date:	Thursday, September 17, 2009	Sheet 37 of 49





[PWM]



AO1718 $R_{dson} = 3 \sim 4.3m\Omega$

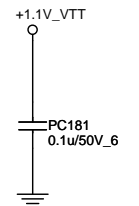
$L(\text{ripple current})$
 $= (19 - 1.05) * 1.05 / (1\mu * 272k * 19)$
 $\sim 3.64A$

$4.3m * 15 = RILIM * 20\mu A$
 $RILIM = 3.24K (3.22K)$

BOM change notice

Arrandale (1.05V) $R1 = 4.02K (CS24023F928)$
 Clarksfield(1.1V) $R1 = 4.75K (CS24753F919)$

5/4
 PR157 change to 4.75K

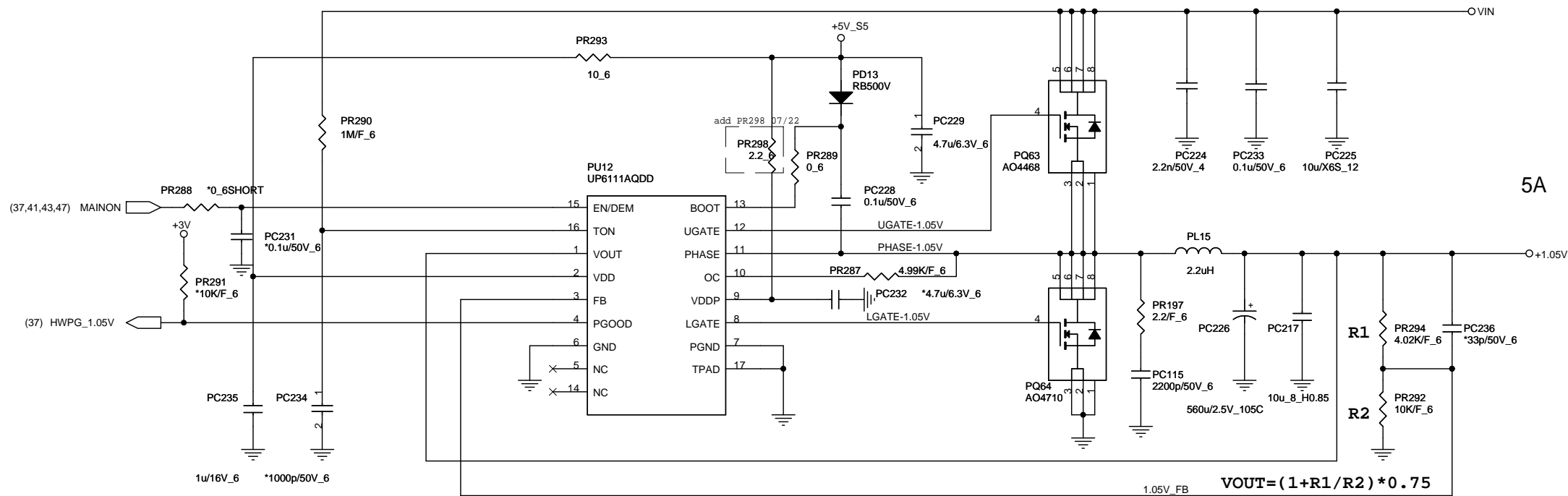


Quanta Computer Inc.

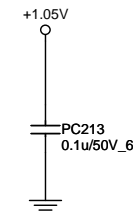
PROJECT : ZY9B

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date:	Thursday, September 17, 2009	Sheet 41 of 49

[PWM]

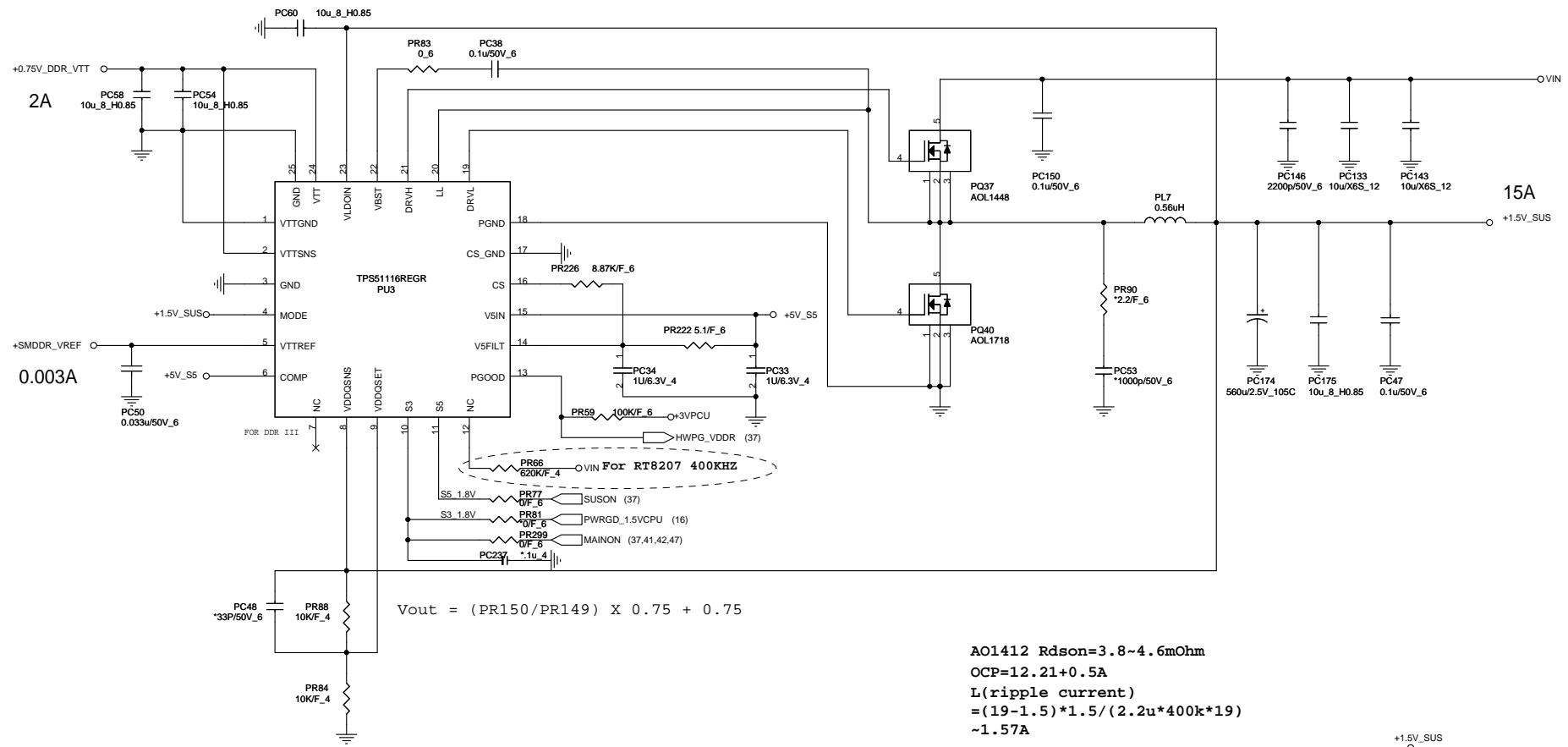


AO4710 $R_{dson} = 11.8 \sim 14.2m\Omega$
 OCP=7.2-0.8A
 $L(\text{ripple current})$
 $= (19 - 1.05) * 1.05 / (2.2u * 272k * 19)$
 $\sim 1.6577A$
 $14.2m * 7 = RILIM * 20uA$
 $RILIM = 4.99K (4.97K)$

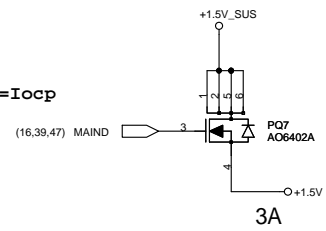
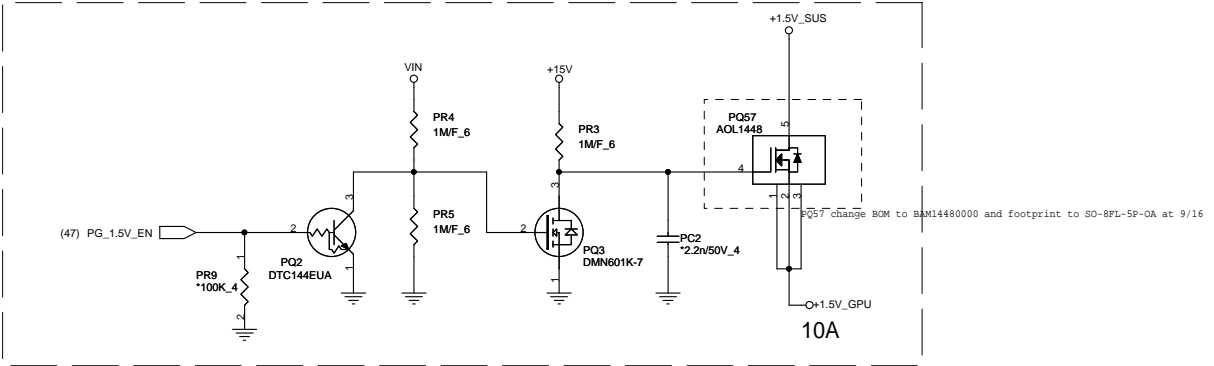


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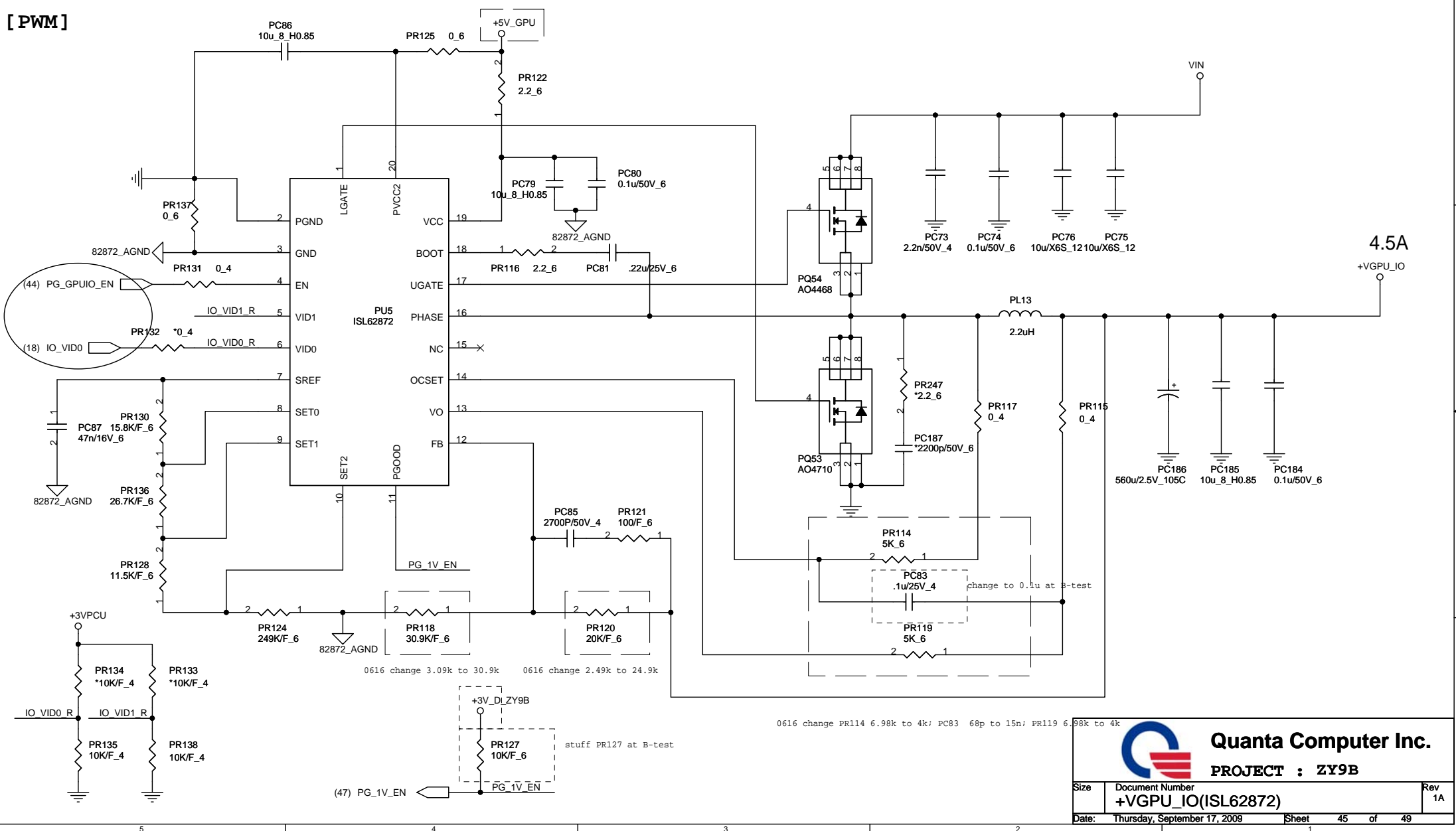
Size	Document Number	Rev
	+1.05V(UP6111AQDD)	1A
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A01412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*19)
~1.57A
4.6m*19=RILIM*10uA
RILIM=8.74K --- 8.87K
(10u*PR35)/Rdson+Delta_I/2=Iocp



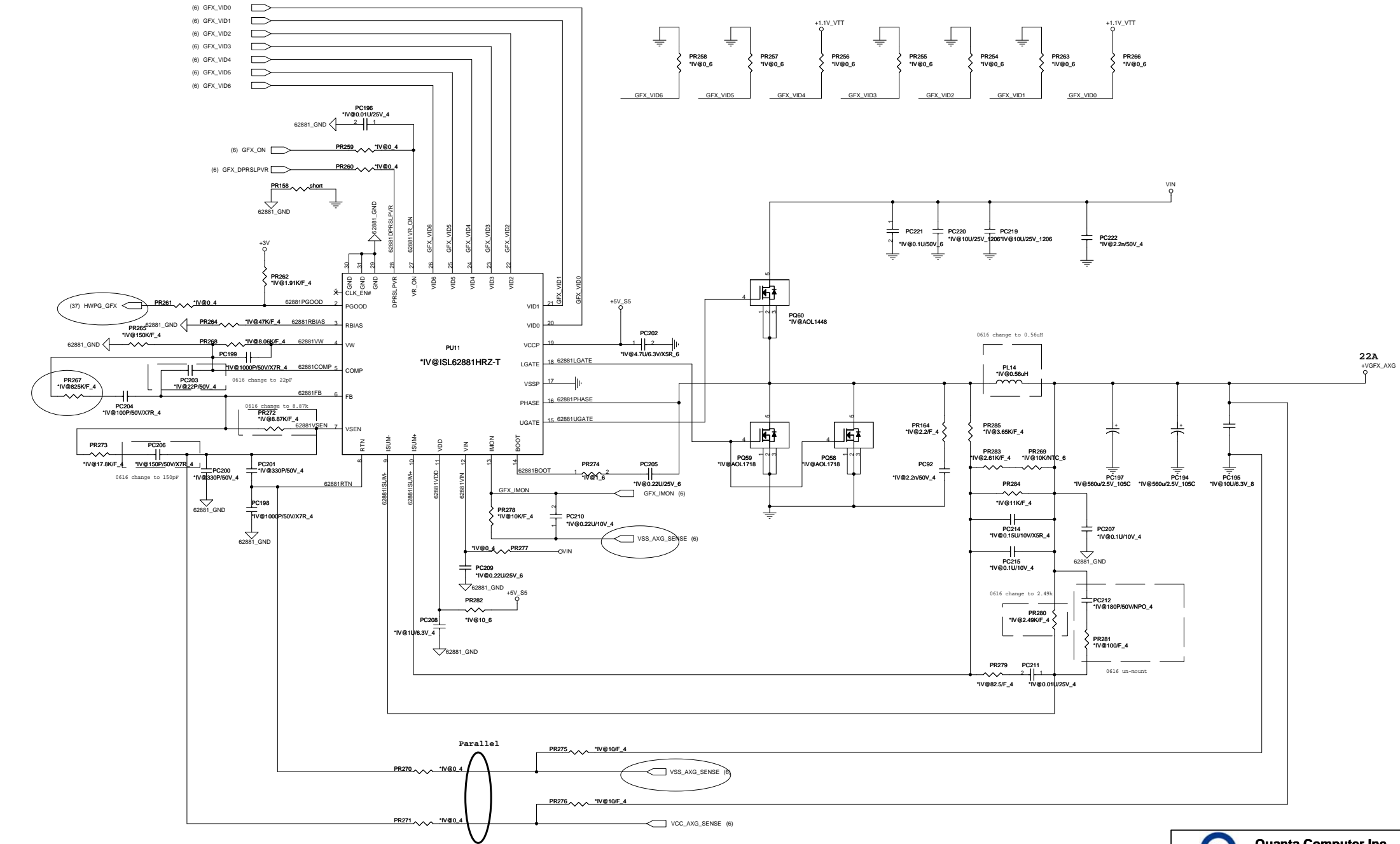
[PWM]



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Size	Document Number	Rev
	+VGPU_IO(ISL62872)	1A
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1. Level 1 Environment-related Substances should NEVER be used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

【PWM】

